ABSTRACT:

This report defines the commonly used two port parameters of generalized linear electrical networks and discusses the theory that underpins two port parameter models. It develops two port circuit analysis methods for evaluating the driving point input impedance, the driving point output impedance, the transfer function, the loop gain, and the stability characteristics of simple and relatively complex active and passive two port network architectures. Basic measurement strategies for the various two port parameters are also addressed.
1.0. INTRODUCTION

The majority of linear passive electrical and active electronic systems can be viewed as two port networks. A network port consists of two electrical terminals, thereby suggesting that a two port network has two readily accessible pairs of electrical terminals. One of these terminal pairs is the input port, to which a known signal voltage or current is applied. The network of interest processes this input voltage or current to produce a desired or designable response at the second of the two network pairs, which is called the output port. The theories and analytical techniques indigenous to basic circuit theory allow the output response of a two port network to be related to its applied input energy as a function of the volt-ampere characteristics of the individual branches embedded in the network. Although this direct formulation of the output response-to-input signal relationship is systematic, three engineering issues limit the utility of this straightforward analytical strategy.

One of the foregoing engineering issues derives from the sheer topological complexity of practical circuits. A useful circuit, and particularly a useful electronic circuit, may contain hundreds or even thousands of branch elements. The immediate effect of this ubiquity of electrical elements is an explosion of the required number of equilibrium equations that must be solved simultaneously to forge the desired input-to-output (I/O) transfer relationship. Manual solution is therefore rendered daunting, if not impossible, thereby encouraging the use of the omnipresent computer. But neither cumbersome manual analyses nor computationally efficient computer-based numerical solutions are likely to inspire the engineering design insights whose assimilation is, in fact, the fundamental goal of circuit analysis.

A second shortcoming of direct circuit analyses is that the electrical characteristics of many internal network branches may not be well defined or clearly understood. This issue is especially nontrivial when the network in question contains active elements, such as bipolar junction transistors (BJTs) and metal-oxide-semiconductor field effect transistors (MOSFETs), that are incorporated to process electrical signals at high speeds. In such an event, electrical responses are vulnerable to stray capacitances, parasitic lead inductances, device processing uncertainties, and undesirable electromagnetic coupling from proximately positioned circuits. To be sure, mathematical models of active elements and the aforementioned second order electrical phenomena can be constructed. But in the interest of analytical tractability, these macromodels are invariably simplified to an extent that virtually ensures inaccuracies in, or even miscomprehension of, the fruits of analysis.

A final point of contention is the superfluous technical information generated as an implicit byproduct of conventional mesh and nodal analyses. The application of the Kirchhoff voltage law (KVL) and the Kirchhoff current law (KCL) produces, in addition to the desired output response, all node and branch voltages and all mesh and loop currents intrinsic to the network undergoing examination. But in many applications, such as active filters that exploit commercially available operational amplifiers (op-amps) or application specific high performance amplifiers, the only engineering concern is the electrical relationship established between the I/O ports of the filter. This relationship can be forged without an explicit awareness of the voltages and currents established within the utilized amplifiers. Indeed, the overall I/O filter transfer function and other performance metrics can be deduced as a function of only electrical properties gleaned from measurements executed at the I/O ports of these amplifiers. These electrical properties, or two port parameters, are admittedly nonphysical entities in that they generally cannot be cast in terms of the physically sound phenomenology that underlies the
electrical nature of observable I/O characteristics. Nonetheless, they are useful because they do derive from reproducible port measurements, and they do conduce the formulation of an analytically unambiguous overall network response.

2.0. FUNDAMENTAL TWO PORT CONCEPTS

Figure (1) abstracts a generalized linear two port electrical network. The input port is formed by the terminal pairs, 1–2, while the output port, which is terminated in an arbitrary load impedance, $Z_l$, is the terminal pair, 3–4. It is presumed that no energy sources lie within the two port network, which implies that if any energy storage elements are embedded therein, zero state conditions apply. Energy is therefore applied to the two port system at only its input port. In Figure (1a), this energy is represented by a Thévenin equivalent circuit comprised of the signal source voltage, $V_s$, and its internal series impedance, $Z_s$. Alternatively, the applied energy can be modeled as the Norton topology depicted in Figure (1b), where the Norton, or short circuit, equivalent current, $I_s$, is

$$ I_s = \frac{V_s}{Z_s}. $$

Because of input signal excitation, a voltage, $V_1$, is established across the input port, a current, $I_1$, flows into this port, a current, $I_2$ flows into the output port, and a voltage, $V_2$, is developed across the output port. Obviously, current $I_2$ and voltage $V_2$ are constrained by the Ohm’s law relationship,

$$ I_2 = -\frac{V_2}{Z_l}. $$

2.1. INPUT PORT MODEL

Because the two port abstraction in Figure (1) is a linear network, both the input port defined by the terminal pair, 1–2, and the output port comprised of terminal pair 3–4 can be modeled by Thévenin or Norton equivalent circuits. Since no energy sources appear in either the
linear network or in the load that terminates the output port, the Thévenin and Norton equivalent circuits of the input port are identical. As is depicted in Figures (2a) and (2b), these equivalent circuits consist of a two terminal impedance, say $Z_{in}$, which is logically termed the input impedance “seen” by the signal source circuit. Alternatively, $Z_{in}$ is often termed the “driving point input impedance.” The phrase, “driving point,” signifies that the impedance properties of the input port are modeled or measured under actual load conditions, as opposed to constraints that stipulate a specific value, say 50 ohms, zero ohms (a short circuit), or infinity ohms (an open circuit), of the load impedance, $Z_{l}$.

![Fig. (2).](image)

An inspection of either of the diagrams in Figure (2) suggests that the input impedance at hand is

$$Z_{in} = \frac{V_1}{I_1},$$

which is equivalent to the stipulation,

$$Z_{in} = \lim_{Z_s \to 0} \left( \frac{V_s}{I_1} \right).$$

Equation (4) is a potentially useful alternative to (3) in that a KVL relationship written around the mesh containing the network input port is invariably required to deduce the transfer properties of the two port system. Accordingly, the input port equation of equilibrium written to discern the I/O transfer properties of the considered two port network can be massaged in accordance with (4) to evaluate the driving point input impedance as well.

In terms of the applied signal excitation, the current, $I_1$, flowing into the input network port is

$$I_1 = \frac{V_s}{Z_s + Z_{in}} = \left( \frac{Z_s}{Z_s + Z_{in}} \right) I_s,$$

while the voltage, $V_1$, developed across the input port is

$$V_1 = \left( \frac{Z_{in}}{Z_{in} + Z_s} \right) V_s = \left( Z_{in} || Z_s \right) I_s.$$
As expected, (5) confirms a null input current when the input port emulates an open circuit \((Z_{in} = \infty)\) and an input current identical to the Norton equivalent signal source current when the input port behaves as a short circuit \((Z_{in} = 0)\). This is to say that the current drawn from the signal source by the two port system is maximized at \(I_s\) under a short circuit input port condition and minimized to zero under an open circuit input port environment. On the other hand, (6) shows that the input port voltage, \(V_1\), is maximized to a value that equals the Thévenin source voltage when \(Z_{in}\) is infinitely large, while \(V_1\) reduces to zero when the input port is a short circuit.

It is interesting to note that at the extremes of a short circuited input port, for which the input port voltage collapses to zero, and an open circuited input port, where the input port current is null, zero power is transferred from the signal source to the subject input port. For all other input port impedance conditions, where neither input port voltage \(V_1\) nor input port current \(I_1\) is zero, the power delivered to the port is nonzero. It is hardly a leap of faith to surmise that for some intermediate, nonzero and finite, value of the driving point input impedance, \(Z_{in}\), the power transferred between the source and the input port is maximized. It can be demonstrated that maximum signal power is indeed transferred to the input terminal pair of a linear two port network when the driving point impedance is conjugately matched to the Thévenin source impedance; that is, \(Z_{in} = Z_s^*\). This so-called match terminated condition, for which neither the input port current nor the input port voltage is either maximal or minimal, is a routine design criterion in high performance electronic systems implemented to process extremely low level source signals. An example of such a system is the ubiquitous cellular telephone. The source signal produced by the antenna in these telephones is often characterized by a very small Thévenin equivalent voltage source. The anemic amplitude of this signal voltage places it at risk of being masked by unavoidably present electrical noise or parasitic electromagnetic energy. To minimize the risk of “losing” this signal and thus, to maximize the probability of signal capture, the input port impedance of the two port amplifier to which the antenna is coupled is almost always designed to match terminate to the antenna, thereby ensuring the transfer of maximum signal power for subsequent amplification and other requisite processing.

2.2. OUTPUT PORT MODELS

The output port model of the network in Figure (1) is marginally more complicated than is the input port model because energy is supplied to the output terminal pair, 3–4, by the signal source voltage, \(V_s\). Specifically, the Thévenin equivalent output port circuit is not a simple impedance element. Instead, it consists of the series interconnection of the driving point output impedance, \(Z_{out}\), and a voltage source, say \(V_{2o}\), whose value is the open circuit (meaning \(Z_l = \infty\)) value of the voltage response evidenced across the output port as a result of the applied input port signal energy. Equivalently, the output port can be represented as a Norton topology consisting of \(Z_{out}\) in shunt with the short circuit (meaning \(Z_l = 0\)) value, say \(I_{2o}\), of the output port current, \(I_2\). These assertions are effectively summarized by Figure (3), which confirms an output port voltage, \(V_2\), given by

\[
V_2 = \left(\frac{Z_l}{Z_l + Z_{out}}\right)V_{2o} = -(Z_l || Z_{out})I_{2o},
\]

and an output port current, \(I_2\), of
Note that maximum output port voltage is achieved for \( Z_l = \infty \) and, as expected, this maximum response is the Thévenin output voltage, \( V_{2o} \). Moreover, the maximum output current is the Norton current, \( I_{2o} \), which is realized for \( Z_l = 0 \).

Since the network undergoing modeling is a linear circuit, the Thévenin output voltage, \( V_{2o} \), as well as the Norton output current, \( I_{2o} \), is proportional to every branch and node variable in the considered two port system. Thus, for example, \( V_{2o} \) is linearly related to the source voltage, \( V_s \), the input port voltage, \( V_1 \), the input port current, \( I_1 \), the Norton source current, \( I_s \), and so forth. An analogous statement applies to \( I_{2o} \). It is useful to capitalize on these observations through an exploitation of gain and transfer relationships commonly used to define the electrical properties of two port configurations. For example, and with reference to Figure (1), the voltage gain, \( A_v \), of the system is

\[
A_v = \frac{V_v}{V_s},
\]

and the forward transimpedance, \( Z_f \), which defines the effect exerted on output port voltage by input signal current, is

\[
Z_f = \frac{V_2}{I_s}.
\]

Since the Thévenin output port voltage is the open circuit value of said port voltage, it is hardly an analytical stretch to define a “Thévenin voltage gain,” \( A_{v0} \), and a “Thévenin forward transimpedance,” \( Z_{f0} \), in accordance with

\[
A_{v0} = \left. \frac{V_v}{V_s} \right|_{Z_l=\infty} \equiv \frac{V_{2o}}{V_s},
\]

and

\[
I_2 = -\frac{V_{2o}}{Z_l + Z_{out}} = \left( \frac{Z_{out}}{Z_{out} + Z_l} \right) I_{2o}.
\]
\[ Z_{fo} = \frac{V_2}{I_s} \bigg|_{Z_I = \infty} \equiv \frac{V_{2o}}{I_s}. \]  

Similarly, if the forward transadmittance, \( Y_f \), and the current gain, \( A_i \), derive from the respective transfer relationships,

\[ Y_f = \frac{I_2}{V_s} \]  

and

\[ A_i = \frac{I_2}{I_s} \]  

\[ Y_{fo} = \frac{I_2}{V_s} \bigg|_{Z_I = 0} \equiv \frac{I_{2o}}{V_s} \]  

is the “Norton forward transadmittance,” and

\[ A_{io} = \frac{I_2}{I_s} \bigg|_{Z_I = 0} \equiv \frac{I_{2o}}{I_s} \]  

**Fig. (4).** (a). Thévenin Output Port Model With Thévenin Voltage Cast As A Proportionality Of The Signal Source Voltage, \( V_s \). (b). Thévenin Output Port Model With Thévenin Voltage Cast As A Proportionality Of The Signal Source Current, \( I_s \). (c). Norton Output Port Model With Norton Current Cast As A Proportionality Of The Signal Source Voltage, \( V_s \). (d). Norton Output Port Model With Norton Current Cast As A Proportionality Of The Signal Source Current, \( I_s \).
represents the “Norton current gain.” Equations (11), (12), (15), and (16) lead to the alternative output port models delineated in Figure (4). One satisfying aspect of these alternate equivalents is that they each underscore $Z_{out}$ as a bona fide Thévenin impedance established at the output port of the generalized network in Figure (1). This statement follows from the fact that a Thévenin impedance at any node pair of a linear network is always computed under the condition of null independent sources of excitation. Since the original system in Figure (1) has but a single independent source of energy—in particular, $V_s$ or $I_s$—that setting $V_s$ or $I_s$ to zero casts $Z_{out}$ as an impedance directly incident with the output terminal pairs of the original two port network.

2.3. TWO PORT PARAMETERS OF IDEAL AMPLIFIERS

The preceding subsection of material leads directly to a compact disclosure of the volt-ampere relationships of idealized two port amplifiers, whose characteristics are often exploited in first order analyses of filters, cascaded gain stages, and other types of analog signal processors. Moreover, the mathematical interpretation of the volt-ampere equations of these idealized electronic structures serve as an excellent means of introducing more general two port relationships, which are addressed in subsequent sections of material. To these ends, four types of amplifiers merit attention.

2.3.1. IDEAL VOLTAGE AMPLIFIER

The ideal voltage amplifier in Figure (5a), which behaves electrically as a voltage controlled voltage source (VCVS), is characterized by infinitely large input impedance, zero output impedance, and constant, frequency independent, open circuit (or Thévenin) voltage gain. At low signal frequencies, the electrical signature of commercially available operational amplifiers emulates that of an ideal voltage amplifier. Recalling the generalized input port and output port models of Figures (2a) and (4a), respectively, Figure (5b) straightforwardly contrived as the relevant two port equivalent circuit. In the latter diagram, the infinitely large input impedance allows an exploitation of the fact that the input port voltage, $V_1$, and the signal source voltage, $V_s$, are identical. The model at hand clearly shows that the input port current, $I_1$, is zero and the output port voltage, $V_2$, is $A_{vo}V_1$. It follows that the port variables of the ideal voltage amplifier interrelate in accordance with the matrix volt-ampere expression,

$$
\begin{bmatrix}
I_1 \\
V_2
\end{bmatrix} =
\begin{bmatrix}
0 & 0 \\
A_{vo} & 0
\end{bmatrix}
\begin{bmatrix}
V_1 \\
I_2
\end{bmatrix}.
$$

(17)

It is worthwhile interjecting that the output voltage, $V_2$, and the input port voltage, $V_1$, are in phase with one another if $A_{vo} > 0$. For $A_{vo} < 0$, the ideal voltage amplifier is said to be a phase inverting amplifier.

In (17), observe that input port current $I_1$ and output port voltage $V_2$ are cast as dependent electrical variables, while input port voltage $V_1$ and output port current $I_2$ serve as independent variables. In view of this codification of network variables, the four parameters (three of which happen to be zero in this specific case) in the $2\times2$ matrix on the right hand side of (17) are traditionally called the hybrid $g$–parameters of the two port network under consideration. The subject matrix itself is termed the $g$–parameter matrix of the considered network.
2.3.2. IDEAL TRANSIMPEDANCE AMPLIFIER

Figure (6a) abstracts an ideal transimpedance amplifier, the electrical characteristics of which emulate those of a current controlled voltage source (CCVS). As is suggested by its equivalent circuit in Figure (6b), the ideal transimpedance amplifier has zero input impedance, zero output impedance, and a frequency invariant forward transresistance, $R_{fo}$. Transimpedance amplifiers are generally formed by coalescing a phase inverting voltage amplifier with appropriate negative feedback. They are commonplace in optoelectronic sensor and communication networks, for which the signal source is a current produced by a reverse biased, and thus high source impedance, photodiode.

\[
\begin{align*}
I_s & \rightarrow Z_s \rightarrow V_i \\
& \rightarrow I_1 \rightarrow V_2 \\
& \rightarrow Z_l \\
& \rightarrow I_2 \rightarrow V_1 \\
I_3 & \rightarrow Z_s \rightarrow V_i \\
& \rightarrow I_1 \rightarrow V_2 \\
& \rightarrow Z_l \\
& \rightarrow I_2 \rightarrow V_1 
\end{align*}
\]

Fig. (5). (a). Voltage-Driven Ideal Voltage Amplifier Terminated At Its Output Port In A Load Impedance, $Z_l$. (b). The Two Port Equivalent Circuit Of The Terminated Amplifier System In (a).

\[
\begin{align*}
I_s & \rightarrow Z_s \rightarrow V_i \\
& \rightarrow I_1 \rightarrow V_2 \\
& \rightarrow Z_l \\
& \rightarrow I_2 \rightarrow V_1 \\
I_3 & \rightarrow Z_s \rightarrow V_i \\
& \rightarrow I_1 \rightarrow V_2 \\
& \rightarrow Z_l \\
& \rightarrow I_2 \rightarrow V_1 
\end{align*}
\]

Fig. (6). (a). Current-Driven Ideal Transimpedance Amplifier Terminated At Its Output Port In A Load Impedance, $Z_l$. (b). The Two Port Equivalent Circuit Of The Terminated Amplifier System In (a). Note That Zero Input Impedance Forces The Input Port Current, $I_1$, To Be Identical To The Signal Source Current, $I_s$. 

The model in Figure (6b) confirms an input port voltage, $V_1$, of zero and an output port voltage, $V_2$, of $R_{fo}I_1$. Accordingly, the port variables of the ideal transimpedance amplifier derive from the matrix volt-ampere expression,

$$
\begin{bmatrix}
  V_1 \\
  V_2
\end{bmatrix} =
\begin{bmatrix}
  0 & 0 \\
  R_{fo} & 0
\end{bmatrix}
\begin{bmatrix}
  I_1 \\
  I_2
\end{bmatrix}.
$$

(18)

With input voltage $V_1$ and output voltage $V_2$ serving as dependent variables and input current $I_1$ and output current $I_2$ used as independent electrical variables, the square matrix on the right hand side of (18) is the z-parameter matrix of the network undergoing investigation. Moreover, the four elements within this matrix are known as the open circuit impedance, or more simply, the z–parameters, of the network.

### 2.3.3. Ideal Transadmittance Amplifier

The ideal transadmittance amplifier offered in Figure (7a) functions as a voltage-controlled current source (VCCS). As is confirmed by the model given in Figure (7b), it is effectively the dual of the ideal transimpedance amplifier in that it is characterized by infinitely large input impedance, infinitely large output impedance, and a forward transconductance, $G_{fo}$, that is independent of signal frequency. Transadmittance amplifiers are also known as transconductors or operational transconductor amplifiers and find utility in wideband electronics realized in high-speed current mode technology. They also comprise the circuit foundation for analog integrators, which, in turn, are used to realize active biquadratic filters, inductorless oscillators, and gyrators.

From the equivalent circuit in Figure (7b), it is apparent that the I/O port volt-ampere equations subscribe to

$$
\begin{bmatrix}
  I_1 \\
  I_2
\end{bmatrix} =
\begin{bmatrix}
  0 & 0 \\
  G_{fo} & 0
\end{bmatrix}
\begin{bmatrix}
  V_1 \\
  V_2
\end{bmatrix}.
$$

(19)
With input voltage $V_1$ and output voltage $V_2$ serving as independent variables and input current $I_1$ and output current $I_2$ exploited as dependent electrical variables, the square matrix on the right hand side of (19) becomes the y-parameter matrix of the network undergoing investigation. Moreover, the four elements within this matrix are known as the short circuit admittance, or y-parameters, of the system. Observe that the model in Figure (7b) reflects the subcircuit of Figure (4c), subject to the proviso that the infinitely large input impedance constrains the input port voltage, $V_i$, to be identical to the source voltage, $V_s$.

### 2.3.4. Ideal Current Amplifier

The ideal current amplifier abstracted in Figure (8a) operates as a current-controlled current source (CCCS). This two port network features zero input impedance, infinitely large output impedance, and a forward current gain, $A_{io}$, that is independent of signal frequency. Its resultant electrical model, which is predicated on the structure in Figure (4d), appears in Figure (8b). The most common application of a current amplifier is current buffering (also known as cascoding) in conjunction with the output port of transadmittance amplifiers. In a cascode application, a current amplifier can significantly increase overall circuit bandwidth, particularly if the pragmatic implementation of a transadmittance amplifier results in significant capacitive feedback between the output and input ports of the transadmittance unit.

![Ideal Current Amplifier Diagram](image)

Fig. (8). (a). Ideal Current Amplifier Terminated At Its Output Port In A Load Impedance, $Z_l$. (b). The Two Port Equivalent Circuit Of The Current Amplifier In (a).

The model in Figure (8b) leads to the volt-ampere matrix relationship,

$$
\begin{bmatrix}
V_1 \\
I_2
\end{bmatrix} = \begin{bmatrix}
0 & 0 & I_1 \\
A_{io} & 0 & V_2
\end{bmatrix}.
$$

With input voltage $V_1$ and output current $I_2$ serving as dependent electrical variables and input current $I_1$ and output voltage $V_2$ identified as independent variables, the square matrix on the right hand side of (20) becomes the hybrid h-parameter matrix of the considered amplifier. Moreover, the four elements within this matrix are known as the hybrid h-parameters of the sys-
Because of the short circuit at the network input port, note that the input port current, $I_1$, is identical to the signal source current, $I_s$.

2.4. GENERALIZED TWO PORT PARAMETERS

The abstraction in Figure (1) and the specialized cases summarized by Figures (5) - through- (8) proffer two lessons. The first is that the two types of driving point specifications (input and output impedance or admittance) and the four types of transfer properties (voltage gain, transimpedance, transadmittance, and current gain) can derive from the measurable input and output port voltages ($V_1$ and $V_2$) and the input and output port currents ($I_1$ and $I_2$). The second lesson is that these observable performance metrics can be quantified analytically even if the circuit architecture implicit to the two port configuration of Figure (1) is unknown, inaccessible, or simply too intricate for straightforward mesh or nodal circuit analyses. The upshot of the matter is that if “jumping into the two port box” to execute appropriate analyses is impossible or impractical, only two equilibrium equations can be written. One of these equations focuses on the input port, where the source energy, source impedance, and the input port variables, $V_1$ and $I_1$, reside, while the other addresses the output port, where the load impedance and the output port variables, $V_2$ and $I_2$, prevail. Since only two equations in the four variables, $V_1, I_1, V_2$, and $I_2$, can be written, the formulation of a unique network solution mandates that two of these variables be viewed as independent, and the resultant two be interpreted as dependent, variables. A viable solution also requires that $V_2$ and $I_2$ be related through the branch properties of the load termination, while $V_1$ and $I_1$ must be uniquely constrained by the source excitation and source impedance. The selection of the independent and dependent variable sets is arbitrary, subject to the proviso that the corresponding two port parameters that define the electrical properties of the network are meaningfully definable and measurable.

2.4.1. Hybrid h—Parameters

A hybrid h-parameter model of a linear two port network derives from choosing input port current $I_1$ and output port voltage $V_2$ as independent electrical variables. Resultantly, input port voltage $V_1$ and output port current $I_2$ are dependent variables. Because the two port network undergoing scrutiny is linear, each dependent variable is a linear superposition of the effects of each independent variable. This observation gives rise to the symbolic volt-ampere relationships,

$$
V_1 = h_{11}I_1 + h_{12}V_2 \quad I_2 = h_{21}I_1 + h_{22}V_2
$$

or in matrix format,

$$
\begin{bmatrix}
V_1 \\
I_2
\end{bmatrix} = \begin{bmatrix}
h_{11} & h_{12} \\
h_{21} & h_{22}
\end{bmatrix} \begin{bmatrix}
I_1 \\
V_2
\end{bmatrix}.
$$

Observe that the ideal current amplifier relationship in (20) is a special case of (22); specifically, it is the special case of $h_{11} = 0$, $h_{12} = 0$, $h_{22} = 0$, and $h_{21} = A_{io}$. The h-parameters are viewed as “hybrid” because of their differing dimensional units. To this end, note in (21) and (22) that dimensional consistency requires that $h_{11}$ be an impedance, $h_{22}$ be an admittance, and $h_{12}$ and $h_{21}$ be dimensionless.
A well-known fact of basic linear circuit theory is that an analysis of a linear circuit produces a set of linear equations. It follows that a set of linear equations, such as is postulated by (21) and (22), corresponds to a linear circuit, which becomes known as an electrical model of the phenomenology addressed by the equation set. Circuit modeling is therefore the inverse of circuit analysis; that is, meaningful equations derive from circuit analysis, while ostensibly useful electrical models are premised on pertinent equilibrium equations.

In the case of (21) and (22), the so called h-parameter model, or h-parameter equivalent circuit, of the linear two port network in Figure (1) is the topological structure shown in Figure (9). The subject model mirrors basic linear circuit theory, which stipulates that any port of a linear circuit can be modeled by either a Thévenin or a Norton equivalent circuit. Recall that Thévenin and Norton models for a simple one port configuration are cast in terms of the independent electrical variables that excite that port. In Figure (9), observe that the Norton equivalent output port current, \( h_{21} I_1 \), and the Thévenin equivalent input port voltage, \( h_{12} V_2 \), are respectively proportional to the variables, \( I_1 \) and \( V_2 \), which have been selected as independent electrical variables in the course of formulating the two port equations of equilibrium.

Measurement procedures for the hybrid h-parameters derive directly from (21) or (22). For example, if the output port voltage, \( V_2 \), is clamped to zero, which corresponds to the short circuited output port drawn in Figure (10a),

\[
\begin{align*}
    h_{11} &= \frac{V_1}{I_1} \bigg|_{V_2 = 0} \\
    h_{21} &= \frac{I_2}{I_1} \bigg|_{V_2 = 0}
\end{align*}
\]  

(23)

It follows that \( h_{11} \) represents the short circuit (meaning that the output port is a short circuit) input impedance of the two port undergoing examination, while \( h_{21} \) designates a forward short circuit current gain. Note, therefore, that \( h_{11} \) is a particular value of the driving point input
impedance addressed in conjunction with Figure (2); specifically, $h_{11}$ is the driving point input impedance under the special case of a short circuited termination of the network output port. On the other hand, $h_{21}$ is a measure of the forward gain of the network since it defines a value for the output port current corresponding to a given input port current. More correctly, $h_{21}$ defines the maximum possible forward current gain in view of the fact that a short circuited load termination is certainly conducive to maximal output port current.

![Linear Two Port Network](image)

**Fig. (10).** (a). Measurement Of The Short Circuit Hybrid h-Parameters. (b). Measurement Of The Open Circuit Hybrid h-Parameters.

With $I_1 = 0$, which reflects the open circuited input port diagrammed in Figure (10b), (21) or (22) yield

$$h_{12} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$$

$$h_{22} = \left. \frac{I_2}{V_2} \right|_{I_1=0}$$  \hspace{1cm} (24)

The parameter, $h_{12}$, is termed the reverse voltage gain, or the h-parameter feedback factor, of a two port network. It is literally the maximum possible reverse voltage gain since the condition, $I_1 = 0$, is identical to a no load condition at the input port. A two port network, and particularly an active two port network, is naturally thought of as a system capable of delivering very large $h_{21}$ so that maximal output signal is generated in response to input port excitation. But a portion of the output response can be returned, or fed back, to the input port because of the electrical nature of the devices implicit to the two port network and the manner in which the elements of the two port are laid out or interconnected. Feedback can also be manifested by the electrical nature of the package in which the electronic circuit is embedded. Feedback can be an undesirable phenomenon, as is the case with packaging anomalies and when bipolar and MOS technology transistors are operated at high signal frequencies. It can also be a specific design objective, as when feedback signal flow paths are appended around active subcircuits to optimize overall
circuit response. Regardless of the source of network feedback, parameter $h_{12}$ is its measure in an h-parameter emulation of linear network I/O performance.

Yet another useful interpretation of $h_{12}$ is that of an isolation factor between output and input ports, with the understanding that $h_{12} = 0$ represents perfect isolation and large $h_{12}$ infers poor isolation, and hence good coupling, of the output port -to- the input port. In an attempt to clarify this assertion, observe in Figure (10b) that

$$V_1 = h_{11}I_1 + h_{12}V_2,$$

whence $V_1/I_1$, which is literally the driving point input impedance of the network, is

$$\frac{V_1}{I_1} = h_{11} + h_{12}\left(\frac{V_2}{I_1}\right).$$

In (26), the ratio, $V_2/I_1$, is the forward transimpedance of the circuit undergoing examination. For a fixed input current, $I_1$, this transimpedance function is certainly influenced by the load termination, which supports the output port voltage $V_2$. For example, a short circuited load necessarily renders $V_2 = 0$, whereby (26) confirms an input impedance that is identical to $h_{11}$. This result is certainly synergistic with the definition of $h_{11}$ in (23). But note that the same impedance result, $V_1/I_1 = h_{11}$, is obtained if $h_{12} = 0$. Evidently $h_{12} = 0$ decouples, or isolates, the output port from its input counterpart in the sense that the input port does not respond to any output port voltage perturbation induced by load fluctuations, parasitic signal coupling, or other phenomena.

In an active two port system, it is generally essential to ensure $|h_{21}| >> |h_{12}|$; that is, the magnitude of the maximum possible forward current gain is desirably much larger than the magnitude of the maximum possible reverse voltage gain. This design requirement is clearly satisfied when the I/O ports are perfectly isolated, in which case the subject two port becomes known as a unilateral network. The term, “unilateral,” refers to an ability of a network to transmit signal between I/O ports in only one direction; in this case, from the input port -to- the output port. A passive network can be shown to have $h_{21} = -h_{12}$, which implies $|h_{21}| = |h_{12}|$. Any linear network for which $h_{21} = -h_{12}$ is said to be bilateral, which means that signal can be propagated equally well from input -to- output ports and from output -to- input ports.

Finally, $h_{22}$ in (24) is the open circuit (meaning that the input port is open circuited) output admittance. Parameter $h_{22}$ is the infinitely large source impedance value of the driving point output admittance, $1/Z_{out}$. For $h_{22} = 0$, the output port in Figure (9) emulates an ideal current source.

A measurement complication arises when the two port network undergoing investigation is an active system. This complication stems from the fact that the active devices embedded within an active topology are inherently nonlinear. Fortunately, these devices behave as approximately linear circuit elements when appropriate static voltages and currents, separate and apart from the input signal source, are applied to bias them within the linear regime of their volt-ampere characteristics. Unfortunately, a short circuited output port, which is required in the measurement of parameters $h_{11}$ and $h_{21}$, and an open circuit input port, which is a prerequisite for the determination of parameters $h_{12}$ and $h_{22}$, are likely to upset the requisite biasing. But on the assumption that the test sources appearing in Figure (10) are sinusoids having zero average value, the biasing dilemma can be circumvented by implementing a short circuit with a suffi-
ciently large capacitance and an open circuit with a sufficiently large inductance. Figure (11) portrays these topological modifications to the h-parameter measurement strategy. Note in this figure that the load and source impedances are not removed since the low frequency values of these elements may be exploited in the network biasing scheme.

![Diagram of Two Port Networks](image)

**Fig. (11).** (a). Measurement Of The Short Circuit Hybrid h-Parameters Of A Linear Active Two Port Network. (b). Measurement Of The Open Circuit Hybrid h-Parameters Of A Linear Active Two Port.

Although the test fixturing in Figure (11) is conceptually correct from the perspective of mitigating biasing difficulties, it is unfortunately impractical when applied to most linear circuits, and it is especially inappropriate when applied to broadband or high frequency linear active two port networks. The fundamental problem is that very few linear active networks, and almost no broadband active networks, are unconditionally stable for all possible source and load terminations. This is to say, that the majority of linear active networks display a propensity for parasitic oscillations for certain values of source and load impedances. Since the amplitudes and frequencies of these oscillations are independent of signal source energy, the two port network in question ceases to be a linear network, thereby invalidating all two port analytical disclosures at this juncture. Open circuit source and load ports are especially troublesome, but even short circuit I/O terminations can induce oscillations. For this reason, the h-parameters and other two port parameter sets for active two port networks are rarely measured directly. Instead, these metrics are usually measured indirectly by calculating them as a function of the measured scattering, or S-, parameters [2]-[4]. Like the h-parameters, the S-parameters quantify the driving point, forward transfer, and feedback properties of a two port system. But unlike h- and other two port parameters to be discussed shortly, S-parameters derive under the operating condition of finite, nonzero, and equal source and load impedances that are chosen to ensure that the network under test operates as a stable entity. Invariably, this equal source and load test termination, which is called the measurement reference impedance, is usually 50, 75, or 300 ohms.
EXAMPLE #1:

Figure (12) depicts the low frequency, small signal equivalent circuit of a common emitter bipolar junction transistor amplifier that utilizes an emitter degeneration resistance, $R_e$, to achieve a forward gain that is nominally independent of the transistor current gain parameter, $\beta$. With reference to Figure (1), note that electrical ground is common between the input and output ports so that the port terminals, 2 and 4, are one and the same ground node. Let the amplifier input resistance, $r_i$, be 2.2 KΩ, the transistor output resistance, $r_o$, is 25 KΩ, $\beta = 90$, and $R_e = 80$ Ω. Derive general expressions for, and numerically evaluate, the four h-parameters, $h_{ij}$, of the emitter degenerated configuration.

![Fig. (12). The Small Signal Equivalent Circuit Of The Amplifier Addressed In Example #1.](image)

SOLUTION:

(1). Figure (13a) is the equivalent circuit appropriate for evaluating the short circuit h-parameters, $h_{11}$ and $h_{31}$. In particular, the subject figure is Figure (12) drawn under the condition of a short circuited output port. A KVL equation written for the output port delivers

$$0 = r_o (I_2 - \beta I_1) + R_e \left( I_1 + I_2 \right),$$

whence

$$h_{21} = \frac{I_2}{I_1} = \beta \left( \frac{1 - R_e / \beta r_o}{1 + R_e / r_o} \right) = 89.71 \text{ amps/amp}.$$  

Armed with this result, KVL around the input loop yields

$$V_1 = r_i I_1 + R_e \left( I_1 + I_2 \right) = \left( r_i + R_e \right) I_1 + \beta R_e \left( \frac{1 - R_e / \beta r_o}{1 + R_e / r_o} \right) I_1,$$

from which

$$h_{11} = \frac{V_1}{I_1} = r_i + (\beta + 1) \left( r_o || R_e \right) = 9.46 \text{ KΩ}.$$  

(2). Figure (13b) is the diagram appropriate for the computation of h-parameters $h_{12}$ and $h_{22}$. With $I_1 = 0$, it is clear that

$$V_2 = \left( r_o + R_e \right) I_2$$

$$V_1 = R_e I_2$$
and thus,

\[
\begin{align*}
    h_{22} &= \frac{I_2}{V_2} = \frac{1}{R_e + r_o} = 39.87 \ \mu S \\
    h_{12} &= \frac{V_1}{V_2} = \frac{R_e}{R_e + r_o} = 3.19 \text{ mVolts/Volt}.
\end{align*}
\]

**COMMENTS:** In addition to expediting amplifier modeling and circuit analysis, the h-parameters are seen herewith as highlighting the electrical effects of an appended circuit element (in this case, the emitter degeneration resistance, \( R_e \)). For example, by inspecting the \( R_e = 0 \) (no emitter degeneration) values of the four h-parameters, the following conclusions are drawn. First, emitter degeneration minimally impacts the forward short circuit current gain, \( h_{21} \) and the open circuit output port conductance, \( h_{22} \), provided \( R_e << r_o \). On the other hand, the emitter degeneration resistance substantively increases the open circuit input resistance, \( h_{11} \), and is literally the cause of nonzero isolation, \( h_{12} \), between the input and output amplifier ports.
2.4.2. Hybrid g–Parameters

The independent and dependent electrical variable sets used to define the hybrid g-parameters are the converse of those used in conjunction with the hybrid h-parameters. Specifically, the independent variables for g-parameter modeling are the input port voltage, \( V_1 \), and the output port current, \( I_3 \), thereby rendering the input port current, \( I_1 \), and the output port voltage, \( V_2 \), dependent electrical quantities. From superposition theory,

\[
\begin{bmatrix}
I_1 \\
V_2
\end{bmatrix} =
\begin{bmatrix}
g_{11} & g_{12} \\
g_{21} & g_{22}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
I_2
\end{bmatrix},
\]  

which gives rise to the g-parameter equivalent circuit depicted in Figure (14). Dimensional consistency requires \( g_{11} \) to be an admittance, \( g_{22} \) a resistance, and \( g_{12} \) and \( g_{21} \) both dimensionless. Observe that for the special case of an ideal voltage amplifier, whose volt-ampere equations are given by (17), \( g_{11} = 0 \), \( g_{12} = 0 \), \( g_{22} = 0 \), and \( g_{21} = A_{vo} \).

As with the hybrid h-parameters, the measurement strategy for the hybrid g-parameters derives directly from the defining volt-ampere modeling relationships. To wit, (27) suggests that parameters \( g_{11} \) and \( g_{21} \) are measured or evaluated under an open circuited output port condition, while \( g_{12} \) and \( g_{22} \) evolve from a short circuited input port constraint. Specifically,

\[
\begin{align*}
g_{11} & = \left. \frac{I_1}{V_1} \right|_{I_2 = 0} \\
g_{21} & = \left. \frac{V_2}{V_1} \right|_{I_2 = 0}
\end{align*}
\]

which casts \( g_{11} \) as an open circuit (meaning that the output port is open circuited) input port admittance and \( g_{21} \) as an open circuit forward voltage gain of the two port network. With refer-
ence to Figure (1), $g_{11}$ is the inverse of the input impedance, $Z_{in}$, under the special case of $I_2 = 0$, while $g_{21}$ is the input port -to- output port Thévenin voltage gain. Continuing in (27),

$$g_{12} = \begin{vmatrix} I_1 \\ I_2 \end{vmatrix} \begin{vmatrix} V_{i} = 0 \end{vmatrix}$$

$$g_{22} = \begin{vmatrix} V_2 \\ I_2 \end{vmatrix} \begin{vmatrix} V_{i} = 0 \end{vmatrix}$$

(29)

Thus, $g_{22}$ is the short circuit (meaning that the input port is short circuited) output impedance of the two port. It is, in fact, the output impedance, $Z_{out}$, in Figure (1) under the special case of a short circuit source impedance termination at the input port. Parameter $g_{12}$, like h-parameter $h_{12}$, is a measure of feedback from the output port -to- the input port. Equivalently, $g_{12}$ measures the degree of isolation between input and output network ports. The salient implications of (28) and (29) are summarized topologically by Figure (15).

Fig. (15). (a). Measurement Of The Open Circuit Hybrid g-Parameters. (b). Measurement Of The Short Circuit Hybrid g-Parameters.

At this juncture, two alternatives for the modeling and ultimate analysis of a linear two port network have been documented. If h-parameters are selected as the modeling vehicle, the applicable equivalent circuit is the structure appearing in Figure (9), while if g-parameters are preferred, the applicable model is the topology of Figure (14). When either modeling approach is adopted for a given two port system, both must necessarily predict identical driving point, forward transfer, and feedback properties. This homogeneity constraint implies that the h- and g-parameters are not mutually independent network metrics; that is, the individual h- and g-parameters must be related.

The nature of the interrelationship between the h- and g-parameters of linear two port network is rendered transparent by a comparison of (27) with (22). In particular, the g-parameter matrix on the right hand side of (27) is the inverse of the h-parameter matrix on the right hand side of (22); that is,
\[
\begin{bmatrix}
g_{11} & g_{12} \\
g_{21} & g_{22}
\end{bmatrix}
= \begin{bmatrix}
h_{11} & h_{12} \\
h_{21} & h_{22}
\end{bmatrix}^{-1},
\tag{30}
\]

and conversely,
\[
\begin{bmatrix}
h_{11} & h_{12} \\
h_{21} & h_{22}
\end{bmatrix}
= \begin{bmatrix}
g_{11} & g_{12} \\
g_{21} & g_{22}
\end{bmatrix}^{-1}.
\tag{31}
\]

With
\[
\Delta_h = h_{11}h_{22} - h_{12}h_{21}
\tag{32}
\]
representing the determinant of the h-parameter matrix, (30) requires
\[
\begin{align*}
g_{11} &= \frac{h_{22}}{\Delta_h} \\
g_{22} &= \frac{h_{11}}{\Delta_h} \\
g_{12} &= -\frac{h_{12}}{\Delta_h} \\
g_{21} &= -\frac{h_{21}}{\Delta_h}
\end{align*}
\tag{33}
\]

From (31),
\[
\begin{align*}
h_{11} &= \frac{g_{22}}{\Delta_g} \\
h_{22} &= \frac{g_{11}}{\Delta_g} \\
h_{12} &= -\frac{g_{12}}{\Delta_g} \\
h_{21} &= -\frac{g_{21}}{\Delta_g}
\end{align*}
\tag{34}
\]

where
\[
\Delta_g = g_{11}g_{22} - g_{12}g_{21}
\tag{35}
\]
is the determinant of the g-parameter matrix.
It is interesting to note that although in principle, the selection of the type of parameters exploited to model a two port network is arbitrary, the actual choice may be dictated by network pragmatics. For example, observe in (33) that the g-parameters are not finite, and thus are not numerically deterministic, if the determinant of the h-parameter matrix is zero. Zero determinant defines matrix singularity and thus, g-parameters cannot be defined if the corresponding h-parameter matrix is singular. Moreover, (34) shows that h-parameters cannot be evaluated numerically if the g-parameter matrix is singular, that is if \( \Delta_g = 0 \). It follows that some two port networks, and particularly active two ports, may have an h-parameter modeling representation in lieu of a g-parameter equivalent circuit and vice versa. Actually, it is possible that neither an h-nor a g-parameter model exists, in which case other two port parameter sets must be exploited.

Finally, note that the g-parameter feedback factor, \( g_{12} \), is nominally proportional to its h-parameter counterpart, \( h_{12} \). Similarly, the feedforward parameter, \( g_{21} \), is nominally proportional to \( h_{21} \). Accordingly, both the g-parameter and the h-parameter equivalent circuits are analytically consistent with respect to disclosing the degree of feedback, or isolation, evidenced and also with respect to the degree of feedforward transmission observed.

**EXAMPLE #2:**

Figure (16) is a simplified low frequency, small signal equivalent circuit of a voltage amplifier that exploits feedback via the resistance, \( R_2 \). Let \( R_1 = 9 \, K\Omega \), and \( R_2 = 1 \, K\Omega \), and assume an amplifier output resistance, \( r_o \), of 100 \, \Omega \), and an amplifier open loop gain (gain in the absence of feedback), \( A_o \), of 100. Derive general expressions for, and numerically evaluate, the four g-parameters, \( g_{ij} \), of the feedback amplifier.

![Fig. (16). The Small Signal Equivalent Circuit Of The Amplifier Studied In Example #2.](image)

**SOLUTION:**

(1). Figure (17a), which is the circuit diagram in Figure (16) with an open circuited output port invoked, is the equivalent circuit for evaluating the g-parameters, \( g_{11} \) and \( g_{21} \). By inspection of the input port mesh,

\[
V_I = (R_1 + R_2)I_I,
\]

so that

\[
g_{11} = \frac{I_I}{V_I} = \frac{1}{R_1 + R_2} = 100 \, \mu S.
\]

At the output port of Figure (17a),
Fig. (17). (a). Model Used To Calculate g-Parameters $g_{11}$ and $g_{21}$ In The Circuit Of Figure (16). (b). Model Appropriate For The Calculation Of g-Parameters $g_{12}$ and $g_{22}$ In Figure (16).

\[
V_2 = A_o V + R_2 I_1 = - A_o R_1 I_1 + R_2 I_1 = - \left( A_o R_1 - R_2 \right) \frac{V_1}{R_1 + R_2}.
\]

It follows that

\[
g_{21} = \frac{V_2}{V_1} = - A_o \left( \frac{1 - R_2/A_o R_1}{1 + R_2/R_1} \right) = -89.90 \text{ volts/volt}
\]

(2). Figure (17b) is the relevant equivalent circuit for computing g-parameters $g_{12}$ and $g_{22}$. With $V_1 = 0$, the I/O port currents are constrained by

\[
0 = R_1 I_1 + R_2 \left( I_1 + I_2 \right).
\]

from which,

\[
g_{12} = \frac{I_1}{I_2} = - \frac{R_2}{R_1 + R_2} = -0.10 \text{ amps/amp}
\]

Moreover

\[
V_2 = r_o I_2 - A_o R_1 I_1 + R_2 \left( I_1 + I_2 \right).
\]
Using the preceding result for the current ratio, $I_1/I_2$, it is a simple matter to show that

$$g_{22} = \frac{V_2}{I_2} = r_o + \left( A_o + 1 \right) \left( R_1 \parallel R_2 \right) = 91.0 \ \Omega .$$

**COMMENTS:** The g-parameter model underscores the fact that for the amplifier at hand, feedback resistance $R_2$ results in an enormous boost of the short circuit output resistance. It also lowers the open circuit input conductance. As expected, a feedback resistance of zero incurs no short circuit feedback within the amplifier. Finally, $R_2$ has little impact on the open circuit voltage gain of the amplifier.

### 2.4.3. Short Circuit y-Parameters

When the input port voltage, $V_1$, and the output port voltage, $V_2$, are chosen as independent variables in the course of analyzing a linear two port network, the relevant volt-ampere relationships assume the form,

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} .$$

In (36), for which the circuit-level interpretation is Figure (18), the $y_{ij}$ are called the admittance, or y-, parameters of the two port system undergoing characterization. The $y_{ij}$ are also called the short circuit admittance parameters because each element in the matrix on the right hand side of (36) is an admittance function and is measured under the condition of a short circuited network port. Specifically,

![Fig. (18). The Short Circuit Admittance Parameter Model Of A Linear Two Port Network. Each of the y-parameters, $y_{ij}$, Have Units Of Admittance.](image-url)
\[ y_{11} = \frac{I_1}{V_1} \bigg|_{V_2=0} \]
\[ y_{21} = \frac{I_2}{V_1} \bigg|_{V_2=0} \] (37)

and

\[ y_{12} = \frac{I_1}{V_2} \bigg|_{V_1=0} \]
\[ y_{22} = \frac{I_2}{V_2} \bigg|_{V_1=0} \] (38)

It follows that parameter \( y_{11} \) is the short circuit (meaning that the output port is short circuited) input admittance of the two port network, while \( y_{21} \) is the corresponding short circuit forward transadmittance. Parameter \( y_{11} \) is therefore related to the driving point input admittance or impedance of the network undergoing scrutiny. On the other hand, \( y_{21} \) is a measure of the forward gain. In (38) \( y_{12} \) is seen as a feedback factor, measured herewith as a reverse short circuit (meaning that the input port is short circuited) transadmittance, and \( y_{22} \) is the short circuit output admittance.

Because a two port network study predicated on \( y \)-parameters must produce results that mirror those that derive from investigations based on either \( h \)- or \( g \)-parameters, the \( y_{ij} \) of a linear network are necessarily related to both the \( h_{ij} \) and the \( g_{ij} \) of the same network. For example, compare (22) with (36) to deduce that with a short circuit imposed at the network output port \( (V_2 = 0) \),

\[ y_{11} = \frac{I_1}{V_1} \bigg|_{V_2=0} = \frac{I}{h_{11}} \]
\[ y_{21} = \frac{I_2}{V_1} \bigg|_{V_2=0} = \frac{h_{21}}{h_{11}} \] (39)

As expected, \( y_{21} \), which is the \( y \)-parameter measure of forward signal transmission through a linear network, is proportional to \( h_{21} \), which is the \( h \)-parameter counterpart to this network gain metric. Moreover, recall that \( h_{11} \) is the short circuit input impedance of a linear two port network. It is therefore only fair that \( y_{11} \), which represents the short circuit input admittance, be the inverse of \( h \)-parameter \( h_{11} \). Continuing the comparison between (22) and (36),
Also as expected, the $y$-parameter feedback parameter, $y_{12}$, is directly proportional to the $h$-parameter feedback measure, $h_{12}$. Recalling that $h_{12} = -h_{21}$ for a bilateral two port network, (39) and (40) imply that bilateralness requires $y_{12} = y_{21}$. Despite the fact that both $h_{22}$ and $y_{22}$ measure network output port admittance, $y_{22}$ does not equal $h_{22}$. The reason underlying $y_{22} \neq h_{22}$ is that $h_{22}$ monitors the output port admittance with the input port open circuited, while $y_{22}$ is the output admittance under the condition of a short circuited input port.

An interesting, and often utilitarian alternative to the basic $y$-parameter equivalent circuit in Figure (18) results when (36) is rewritten in the form

\[
\begin{align*}
y_{12} &= \frac{I_1}{V_2} \bigg|_{V_j=0} = -\frac{h_{12}}{h_{11}} \\
y_{22} &= \frac{I_2}{V_2} \bigg|_{V_i=0} = h_{22} - \frac{h_{12}h_{21}}{h_{11}}
\end{align*}
\] (40)
Upon introducing the subsidiary admittance parameters,

\[
\begin{align*}
y_i & \triangleq y_{11} + y_{12} \\
y_r & \triangleq -y_{12} \\
y_f & \triangleq y_{21} - y_{12} \\
y_o & \triangleq y_{22} + y_{12}
\end{align*}
\]  

\hspace{1cm} (42)

which implies the alternative \(y\)-parameter model topology offered in Figure (19a). This \(\pi\)-type structure requires that the original linear two port network operate with a common terminal between its input and output ports; that is, the original configuration is effectively a three terminal, two port system. The alternative structure requires only one dependent generator, portrays \(y_i\) as a shunting input port branch admittance, \(y_o\) as a shunting output port branch admittance, \(y_r\) as an I/O port coupling admittance, and \(y_f\) as an effective forward transimpedance. For the special case of a bilateral two port network, for which \(y_{12} = y_{21}\), \(y_f\) is zero, and the model in Figure (19a) collapses to the true \(\pi\)-type architecture shown in Figure (19b).

**EXAMPLE #3:**

\[\text{Figure (20). Small Signal Model Of A MOSFET Configured To Operate As A Common Source Amplifier. The Model Is The Focus Of Attention In Example #3.}\]
terminal is presumed grounded for small signals), $r_o$ designates the source-drain channel resistance, and finally, $g_m$ is the forward transconductance of the device. Find general expressions for each of the four common source y-parameters, $y_{ij}$. Also, derive a general expression for the short circuit (meaning the drain terminal is short circuited to the source terminal) current gain and the frequency at which the magnitude of this short current gain degrades to unity. If $g_m = 8 \, \text{mS}$, $r_o = 8 \, \text{K}\Omega$, $C_{gs} = 15 \, \text{fF}$, $C_{gd} = 3 \, \text{fF}$, and $C_{db} = 12 \, \text{fF}$, numerically evaluate this unity gain frequency, which is commonly symbolized as $f_T$.

**SOLUTION:**

(1). The good news about this problem is that the model in Figure (20) is identical to that of the generalized topology shown in Figure (19a). By inspection, therefore, and with $y_{ij}$ signifying the conductance value of the resistance, $r_o$,

\[
\begin{align*}
y_i &= sC_{gs} \\
y_r &= sC_{gd} \\
y_o &= g_o + sC_{db} \\
y_f &= g_m
\end{align*}
\]

It follows from (42) that

\[
\begin{align*}
y_{12} &= -y_r = -sC_{gd} \\
y_{11} &= y_i - y_{12} = s\left(C_{gs} + C_{gd}\right) \\
y_{22} &= y_o - y_{12} = g_o + s\left(C_{db} + C_{gd}\right) \\
y_{21} &= y_f + y_{12} = g_m - sC_{gd}
\end{align*}
\]

(2). Extensive circuit analysis is not required for an evaluation of the short circuit current gain. Instead, it is necessary only that $h$-parameter $h_{21}$ be recalled as the short circuit current gain of a linear two port network. From (39),

\[
\frac{y_{21}}{y_{11}} = h_{21},
\]

and using the results of the preceding analytical step,

\[
h_{21} = \frac{g_m - sC_{gd}}{s\left(C_{gs} + C_{gd}\right)}.
\]

(3). The short circuit current gain, $h_{21}$, computed in the preceding solution step indicates the presence of a right half plane zero at a frequency of $g_m/C_{gd}$, which is $2\pi(424.4 \, \text{GHz})$. This extremely large critical frequency is potentially beyond the frequency range of validity of the model in Figure (20) and is likely to be significantly larger than the unity gain frequency, which is to be computed. Accordingly, if the unity gain frequency is indeed much smaller than the frequency of the right half plane zero,

\[
h_{21} \approx \frac{g_m - sC_{gd}}{s\left(C_{gs} + C_{gd}\right)} \approx \frac{g_m}{s\left(C_{gs} + C_{gd}\right)}.
\]
Under steady state sinusoidal signal conditions, \( s \) is replaced by \( j\omega \) in the preceding disclosure, with the result that

\[
h_{21} = \frac{g_m}{j\omega \left( C_{gs} + C_{gd} \right)}.
\]

Clearly, the magnitude of \( h_{21} \) decreases progressively with increasing signal and becomes one at

\[
f_T = \frac{g_m}{2\pi \left( C_{gs} + C_{gd} \right)} = 70.7 \text{ GHz}.
\]

COMMENTS: In this particular example, note that two port parameter theory leads expediently to the analytical and numerical definitions of a commonly invoked figure of merit for MOSFETs; namely, the unity gain frequency, \( f_T \). The computed \( f_T \)-value of better than \( 70 \text{ GHz} \) is quite large and indicative of deep submicron technology devices. However, it is worthwhile interjecting that although \( f_T \) commonly serves as a reasonably useful metric for comparing the high frequency attributes of one transistor against another, it is a less than meaningful metric for MOSFET circuits and systems. The unity gain frequency of an actual circuit that exploits MOSFET technology is invariably much smaller than the transistor \( f_T \) rating. A principal reason for this disparity is that the short circuit basis for enumerating \( f_T \) inherently ignores drain-bulk capacitance. It is also oblivious to the potentially dominant energy storage elements—parasitic or otherwise—embedded within the circuit.

### 2.4.4. INDEFINITE ADMITTANCE PARAMETERS

An interesting and useful extension to the two port \( y \)-parameter concept entails the consideration of the three terminal linear network abstracted in Figure (21). The network at hand is operated as a three port configuration, with each of the three ports supporting a voltage referenced to system ground. At first blush, the subject analytical extension is seemingly trivial since superposition theory allows the matrix expression,

\[
\begin{bmatrix}
I_1 \\
I_2 \\
I_3
\end{bmatrix} =
\begin{bmatrix}
y_{11} & y_{12} & y_{13} \\
y_{21} & y_{22} & y_{23} \\
y_{31} & y_{32} & y_{33}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix},
\]

\[
(43)
\]
to be postulated as the pertinent condensed volt-ampere relationship. To be sure, (43) is a valid generality, but it incorrectly implies that each of the admittance parameter, \( y_{ij} \), is independent of one another. In truth, only four of the nine indicated admittance metrics can be measured or computed independently.

A clarification of the preceding assertion begins be observing that the subject three port network functions essentially as one giant happy node in the sense that the three port currents, \( I_1 \), \( I_2 \), and \( I_3 \), must sum to zero for any and all port voltages, \( V_1 \), \( V_2 \), and \( V_3 \). From (43), this constraint means that
Fig. (21). Schematic Abstraction Of A Linear Three Port Network. Note That The Second Terminal Of Each Of The Three Ports Is System Ground.

\[
\begin{align*}
y_{11} + y_{21} + y_{31} & = 0 \\
y_{12} + y_{22} + y_{32} & = 0 \\
y_{13} + y_{23} + y_{33} & = 0
\end{align*}
\]

which is tantamount to requiring that the sum of the elements in each of the three columns in the 3x3 matrix on the right hand side of (43) be zero. An additional parametric constraint is manifested through the consideration of the special circumstance in which all three network port voltages are identical. In this case, no potential difference exists and thus no energy is applied, between any two of the three network terminals. Under the condition of null differential applied energy implied by \( V_1 = V_2 = V_3, I_1 = I_2 = I_3 = 0 \) if and only if

\[
\begin{align*}
y_{11} + y_{12} + y_{13} & = 0 \\
y_{21} + y_{22} + y_{23} & = 0 \\
y_{31} + y_{32} + y_{33} & = 0
\end{align*}
\]

Accordingly, the admittance elements in each of the three rows of the 3x3 matrix in (43) must, like the elements in each column, sum to zero. The immediate ramification of this disclosure is that the generalized volt-ampere relationship in (43) is expressible as

\[
\begin{bmatrix}
I_1 \\
I_2 \\
I_3
\end{bmatrix} =
\begin{bmatrix}
y_{11} & y_{12} & -(y_{11} + y_{12}) \\
y_{21} & y_{22} & -(y_{21} + y_{22}) \\
-(y_{11} + y_{21}) & -(y_{12} + y_{22}) & (y_{11} + y_{12} + y_{21} + y_{22})
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix}.
\]

The 3x3 matrix on the right hand side of this relationship is termed the indefinite admittance matrix of the three port shown in Figure (21). For an \( n \)-terminal linear network, an \( nxn \) indefinite...
 Infinite admittance matrix can be constructed straightforwardly in terms of the admittance parameters of the reduced \((n-1)\)–terminal configuration simply by invoking the constraints of zero row and column sums in the resultant \(nxn\) matrix.

In an effort to garner appreciation for the indefinite admittance matrix concept, consider the case in which the four admittance parameters of the two port network resulting from \(V_3 = 0\) have been measured or otherwise evaluated. The resultant volt-ampere expression, is (36), where it is tacitly assumed that the port voltages, \(V_1\) and \(V_2\), are referenced to electrical ground. It follows that volt-ampere characteristics when \(V_3\) is nonzero is (46), where again, all port voltages are presumed referenced to electrical ground. Suppose now that the network in Figure (21) is operated with terminal 2 grounded and with nonzero \(V_1\) and \(V_3\). Since \(V_2 = 0\), the second column of matrix elements on the right hand side of (46) can be discarded without loss of any information. Moreover, since \((I_1 + I_2 + I_3) = 0\) is guaranteed by the construction of the indefinite admittance matrix, the analytical information surrounding current \(I_2\), which flows into the grounded second port, is superfluous. It follows that the second row of matrix elements in (46) can also be discarded, thereby rendering

\[
\begin{bmatrix}
I_1 \\
I_3
\end{bmatrix} = \\
\begin{bmatrix}
y_{11} & -(y_{11} + y_{12}) \\
-(y_{11} + y_{21}) & (y_{11} + y_{12} + y_{21} + y_{22})
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_3
\end{bmatrix}
\]

as the applicable system of volt-ampere equations. Note that this system of equilibrium equations results exclusively from the characterization of the original system operated with terminal 3 grounded and does not require the execution of any substantive new analyses.

**EXAMPLE #4:**

Recall Figure (20) as a small signal model of a MOSFET operated as a common source amplifier. Consider now the schematic diagram of Figure (22a), which depicts the same MOSFET operated in a common drain (also referred to as a source follower) configuration. Determine general expressions for each of the four common drain \(y\)-parameters, \(y_{11}, y_{13}, y_{31},\) and \(y_{33}\). The MOSFET model parameters remain \(g_m = 8\ mS, r_o = 8\ K\Omega, C_{gs} = 15\ fF, C_{gd} = 3\ fF,\) and \(C_{db} = 12\ fF\).

**SOLUTION:**

(1). The parameters, \(y_{11}, y_{12}, y_{21},\) and \(y_{22}\), for the common source circuit have been determined in Example #2. For convenience, they are repeated herewith. Recall that \(g_o = 1/r_o\).

\[
\begin{align*}
y_{11} &= s(C_{gs} + C_{gd}) \\
y_{12} &= -sC_{gd} \\
y_{21} &= g_m - sC_{gd} \\
y_{22} &= g_o + s(C_{db} + C_{gd})
\end{align*}
\]

(2). The parameters for the common drain circuit in Figure (22a) derive directly from the foregoing results and (47). Specifically,
Fig. (22). (a). Small Signal Equivalent Circuit Of A MOSFET Oriented Toward Common Drain Signal Processing. The Circuit Is Addressed In Example #4. (b). The Resultant y-Parameter Model Of The Common Drain Circuit In (a).

\[
\begin{align*}
    y_{11} &= s\left(C_{gs} + C_{gd}\right) \\
    y_{13} &= -\left(y_{11} + y_{12}\right) = -sC_{gs} \\
    y_{31} &= -\left(y_{11} + y_{21}\right) = -\left(g_m + sC_{gs}\right) \\
    y_{33} &= y_{11} + y_{12} + y_{21} + y_{22} = g_m + g_o + s\left(C_{gs} + C_{db}\right)
\end{align*}
\]

**COMMENTS:** The resultant y-parameter equivalent circuit is offered in Figure (22b). This model shows that the output impedance of the considered source follower is small, even at low signal frequencies, because of the resistance, \(1/g_m\), that appears directly across the output port.

### 2.4.5. **Open Circuit z–Parameters**

The use of open circuit impedance parameters is premised on selecting the input port current, \(I_1\), and the output port current, \(I_2\), as independent electrical variables in the two port system of Figure (1). The upshot of this selection is the volt-ampere matrix expression

\[
\begin{bmatrix}
    V_1 \\
    V_2
\end{bmatrix} =
\begin{bmatrix}
    z_{11} & z_{12} \\
    z_{21} & z_{22}
\end{bmatrix}
\begin{bmatrix}
    I_1 \\
    I_2
\end{bmatrix},
\]

where the \(z_{ij}\) are the network open circuit impedance parameters, or z–parameters. The equivalent circuit corresponding to (48) is shown in Figure (23) and is seen to exploit Thévenin’s theorem at both the input and output ports.
The Open Circuit Impedance Parameter Model Of A Linear Two Port Network. Each of the z-parameters, $z_{ij}$, Have Units Of Impedance.

The designation of the z-parameters as open circuit impedances follows from the parametric measurement strategy implied by (48). For example

$$z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2 = 0}$$

$$z_{21} = \left. \frac{V_2}{I_1} \right|_{I_2 = 0}$$

whence $z_{11}$ is the open circuit (meaning an open circuited output port) input impedance of the linear two port network. Moreover, $z_{21}$ is seen as the open circuit transimpedance of the two port system. Thus, like $h_{11}$, $g_{11}$, and $y_{11}$, $z_{11}$ influences the input impedance of the network undergoing investigation, and like $h_{21}$, $g_{21}$, and $y_{21}$, $z_{21}$ is a measure of the achievable forward gain. Equation (48) also confirms that

$$z_{12} = \left. \frac{V_1}{I_2} \right|_{I_1 = 0}$$

$$z_{22} = \left. \frac{V_2}{I_2} \right|_{I_1 = 0}$$

Accordingly, $z_{12}$ is the feedback transimpedance under the condition of an open circuited input port, and $z_{22}$ is the open circuit output impedance measured under the same input port open circuit.
A comparison of (48) with (36) suggests immediately that the z-parameter matrix of a two port network is the inverse of the y-parameter matrix of the same system. Assuming that the y-parameter matrix is non-singular and letting

\[ \Delta_y = y_{11}y_{22} - y_{12}y_{21} \]  

(51)

denote the determinant of the y-matrix in (36), the z-parameters relate to their y-parameter counterparts in accordance with

\[ z_{11} = \frac{y_{22}}{\Delta_y} = \frac{1}{y_{11} - \frac{y_{12}y_{21}}{y_{22}}} \]

\[ z_{22} = \frac{y_{11}}{\Delta_y} = \frac{1}{y_{22} - \frac{y_{12}y_{21}}{y_{22}}} \]

\[ z_{12} = -\frac{y_{12}}{\Delta_y} \]

\[ z_{21} = -\frac{y_{21}}{\Delta_y} \]  

(52)

Note that for a bilateral two port, which has \( y_{12} = y_{21} \), \( z_{12} \) is identical to \( z_{21} \).

### 2.4.6. Chain Parameters

The chain parameters, \( c_{ij} \), which are often referred to as the transmission parameters, of the linear two port network in Figure (1) are implicitly defined by the matrix volt-ampere description,

\[
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} =
\begin{bmatrix}
c_{11} & c_{12} \\
c_{21} & c_{22}
\end{bmatrix}
\begin{bmatrix}
V_2 \\
-I_2
\end{bmatrix}.
\]  

(53)

Note that in the c-parameter representation of the volt-ampere characteristics of a linear two port system, the selected independent variables are output port voltage and the negative of output port current, thereby remanding input port voltage and input port current to dependent variable status. In contrast to the four traditional two port parameter representations, the chain parameters are rarely used for circuit modeling purposes. Instead, the c-parameters are used directly in the analysis and design of networks and are especially useful in the design of passive filters comprised of cascaded passive networks.

As usual, the strategy underlying the measurement of the c-parameters follows directly from the defining volt-ampere characteristics. To this end, let the output port of the considered system be open circuited so that the output port current, \( I_2 \), is nulled. Simultaneously, let the input port be voltage-driven to establish an input port voltage, \( V_1 \), and an input port current, \( I_1 \). The resultant test fixturing, shown in Figure (24a), is identical to that of Figure (15a), which is...
used to measure the open circuit hybrid g-parameters, \( g_{11} \) and \( g_{21} \). From (53), \( I_2 = 0 \) suggests that

\[
\begin{align*}
I_2 &= 0 \\
V_2 &= \frac{V_1}{c_{11}}
\end{align*}
\]

From (53), \( I_2 = 0 \) suggests that

\[
\begin{align*}
I_2 &= 0 \\
V_2 &= \frac{V_1}{c_{11}}
\end{align*}
\]

Thus, parameter \( c_{11} \) is dimensionless, and its inverse is the Thévenin voltage gain of the subject two port network. On the other hand, \( c_{21} \) is in units of admittance, and its inverse is the open circuit (meaning that the output port is open circuited), or Thévenin, forward transimpedance of the network. With the output port short circuited, as indicated in Figure (24b), \( V_2 = 0 \) in (53) gives

\[
\begin{align*}
I_2 &= -\frac{I_1}{c_{22}} \\
V_2 &= 0
\end{align*}
\]

Thus, parameter \( c_{11} \) is dimensionless, and its inverse is the Thévenin voltage gain of the subject two port network. On the other hand, \( c_{21} \) is in units of admittance, and its inverse is the open circuit (meaning that the output port is open circuited), or Thévenin, forward transimpedance of the network. With the output port short circuited, as indicated in Figure (24b), \( V_2 = 0 \) in (53) gives

\[
\begin{align*}
I_2 &= -\frac{I_1}{c_{22}} \\
V_2 &= 0
\end{align*}
\]

Clearly, the negative inverse of dimensionless parameter \( c_{22} \) is the Norton current gain of the network. Moreover, the negative inverse of parameter \( c_{12} \) is the Norton forward transadmittance, which renders \( c_{12} \) itself in dimensions of impedance.

As is the case with any other set of two port parameters, the chain parameters can be related to the \( h-, g-, y-, \) or \( z \)-parameters. Since the open circuit impedance parameters are the last
parameters examined and thus still relatively fresh in personal memory, compare (53) with (48). Specifically, observe that

\begin{equation}
\begin{align*}
c_{11} &= \frac{V_1}{V_2} \bigg|_{I_2=0} = \frac{z_{11}}{z_{21}} \\
c_{21} &= \frac{I_1}{V_2} \bigg|_{I_2=0} = \frac{1}{z_{21}}
\end{align*}
\end{equation}

Moreover,

\begin{equation}
\begin{align*}
c_{22} &= -\frac{I_1}{I_2} \bigg|_{V_2=0} = \frac{z_{22}}{z_{21}} \\
c_{12} &= -\frac{V_1}{I_2} \bigg|_{V_2=0} = \frac{z_{11}z_{22} - z_{12}z_{21}}{z_{21}} = \frac{\Delta_z}{z_{21}}
\end{align*}
\end{equation}

From (56) and (57), the determinant, \( \Delta_c \), of the c-parameter matrix is

\begin{equation}
\Delta_c = c_{11}c_{22} - c_{12}c_{21} = \frac{z_{12}}{z_{21}}.
\end{equation}

It follows that the determinant of the chain matrix is unity if the network undergoing study is bilateral; that is if \( z_{12} = z_{21} \). Interestingly enough, the c-matrix is singular if the network it represents is unilateral, which corresponds to a network divorced of feedback (\( z_{12} = 0 \)).

### 2.4.6.1 Input and Output Impedances

Highlighting the fundamental attributes of chain parameters begins by applying the chain matrix concept to the problem of determining the driving point input and output impedances of the original two port system in Figure (1). The input impedance, \( Z_{\text{in}} \), derives from (53) as

\begin{equation}
Z_{\text{in}} = \frac{V_1}{I_1} = \frac{c_{11}V_2 - c_{12}I_2}{c_{21}V_2 - c_{22}I_2}.
\end{equation}

But, since \( V_2 = -Z_lI_2 \), (59) becomes

\begin{equation}
Z_{\text{in}} = \frac{c_{11}Z_l + c_{12}}{c_{21}Z_l + c_{22}}.
\end{equation}

Equation (60) suggests that the driving point input impedance reduces to \( c_{11}/c_{21} \) for the special case of an open circuit load port. When the load termination is a short circuit, \( Z_{\text{in}} \) is \( c_{12}/c_{22} \).
In order to derive an expression for the driving point output impedance, $Z_{out}$, the signal source voltage, $V_s$, is reduced to zero, thereby forcing $V_1 = -Z_s I_1$. This fact and (53) confirm that

$$Z_{out} = \frac{V_2}{I_2} = c_{12} Z_s + c_{12} \cdot \frac{c_{22} Z_s + c_{12}}{c_{21} Z_s + c_{11}}. \quad (61)$$

In the limit of an ideal current source signal drive ($Z_s \rightarrow \infty$), the output impedance approaches $c_{22}/c_{21}$, while for an ideal voltage source signal excitation ($Z_s \rightarrow 0$), $Z_{out}$ collapses to $c_{12}/c_{11}$.

### 2.4.6.2 Voltage Transfer Function

The voltage transfer function, $V_2/V_1$, from the input -to- the output port can be found by using (53) to write

$$V_1 = c_{11} V_2 - c_{12} I_2 = c_{11} - c_{12} \left( -\frac{V_2}{Z_l} \right), \quad (62)$$

whence

$$\frac{V_2}{V_1} = \frac{Z_l}{c_{11} Z_l + c_{12}}. \quad (63)$$

Note that (63) corroborates with (54) in the sense that an infinitely large load impedance delivers a port -to- port voltage gain of $1/c_{11}$. Since the input port voltage, $V_1$, relates to the signal source voltage, $V_s$, as the simple voltage divider,

$$\frac{V_1}{V_s} = \frac{Z_{in}}{Z_{in} + Z_s}, \quad (64)$$

(63) and (59) combine to deliver an overall system voltage gain of

$$\frac{V_2}{V_s} = \frac{Z_l}{\left( c_{11} + c_{21} Z_s \right) Z_l + \left( c_{12} + c_{22} Z_s \right)}. \quad (65)$$

As expected, (65) reduces to (63) when the source impedance, $Z_s$, is zero.

### 2.4.6.3 Cascade Interconnection

The chain parameters and its associated c-parameter matrix are particularly amenable to ascertaining the transfer and driving point characteristics of networks whose architecture is comprised of a cascade of passive or active circuit sections. To this end, consider Figure (25), which depicts a two stage cascade interconnection of two linear two port networks. In terms of the indicated port voltages and port currents, the volt-ampere characteristics of Network $A$ are given by the matrix relationship,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = C_A \begin{bmatrix} V_x \\ -I_{o1} \end{bmatrix}. \quad (66)$$
where $C_A$ is the $2x2$ chain matrix for Network A. Similarly for Network B,

$$
\begin{bmatrix}
V_x \\
I_{i2}
\end{bmatrix} =
C_B
\begin{bmatrix}
V_2 \\
-I_2
\end{bmatrix},
$$

(67)

with $C_B$ denoting the $2x2$ chain matrix for Network B. But since the input port current, $I_{i2}$, to Network B is obviously the negative of the output port current, $I_{o1}$, of Network A, (66) and (67) combine to produce

$$
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} =
C_A
\begin{bmatrix}
V_x \\
-I_{o1}
\end{bmatrix} =
C_A
\begin{bmatrix}
V_x \\
I_{i2}
\end{bmatrix} =
C_A
C_B
\begin{bmatrix}
V_2 \\
-I_2
\end{bmatrix} \neq
C
\begin{bmatrix}
V_2 \\
-I_2
\end{bmatrix},
$$

(68)

where matrix $C$, which is given as,

$$
C = C_A C_B
$$

(69)

is properly interpreted as the $2x2$ chain matrix for the overall cascade interconnection. Obviously, (69) can be extended to embrace a cascade of $n$ network sections, wherein the overall chain matrix becomes simply the ordered product of the chain matrices of the individual members of the cascade. Once the overall chain matrix is evaluated, its elements can be used in conjunction with (60), (61), (63), and (65) to determine the I/O impedances and transfer function of the cascade. Since matrix multiplication is non-commutative ($C_A C_B \neq C_B C_A$), the chain matrix, and thus the performance attributes, of a cascade interconnection of circuits is dependent on the ordering of the individual sections of the cascade. This observation mathematically confirms the transparent engineering fact that the observable network performance depends on the manner in which the individual elements and subsections of the network are connected.

### 2.4.6.4 Series and Shunt Elements

Equation (69) offers an analytical foundation for the systematic evaluation of the transfer and driving point impedance functions of networks comprised of cascade interconnections of passive subcircuits. To wit, consider the impedance, $Z$, connected as shown in Figure (26a) as a branch element in series with an input port having port voltage $V_1$ and port current $I_1$ and an output port, where the pertinent voltage and current variables are $V_2$ and $I_2$, respectively. An application of (54) and (55) to the subject diagram gives a chain matrix, say $C_z$, of

$$
C_z = \begin{bmatrix}
1 & Z \\
0 & 1
\end{bmatrix},
$$

(70)
where the determinant of $C_z$ is seen to be unity, which is as expected in light of the presumed passivity of impedance $Z$. For Figure (26b), which depicts a branch admittance, $Y$, connected as an element that simultaneously shunts both input and output ports,

$$C_y = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}.$$  \hspace{1cm} (71)

It follows that for the tee configuration of Figure (26c), whose structure is a series impedance, $Z_1$, connected in cascade with a shunt admittance, $Y_2$, which in turn is cascaded with a second series impedance, $Z_3$, the network chain matrix, say $C_n$, is

$$C_n = \begin{bmatrix} 1 & Z_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_2 & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_3 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 + Y_2 Z_1 & Z_3 + Z_1 \left(1 + Y_2 Z_3\right) \\ Y_2 & 1 + Y_2 Z_3 \end{bmatrix}.$$  \hspace{1cm} (72)

**EXAMPLE #5:**

The lowpass filter in Figure (27) is terminated at its output port in a resistance, $R_l$. The Thévenin source resistance can either be presumed to be zero or otherwise absorbed into the resistance, $R$. Use chain parameters to derive expressions for the voltage transfer function, $A_v(s) = V_2/V_1$, the driving point input impedance, $Z_{in}(s)$, and the driving point output impedance, $Z_{out}(s)$.

**SOLUTION:**

(1) The chain matrix of the filter follows directly from (72), where $Z_1 = R$, $Y_2 = sC$, and $Z_3 = sL$.

$$C_n = \begin{bmatrix} 1 + sRC & sL + R \left(1 + s^2 LC\right) \\ sC & 1 + s^2 LC \end{bmatrix}.$$
(2). Using (65) with $Z_l = R_l$ and $Z_s = 0$, the voltage gain evaluates as

$$A_v(s) = \frac{V_2}{V_1} = \frac{R_l}{R_l \left(1 + sRC\right) + sL + R \left(1 + s^2LC\right)}$$

$$= \frac{R_l}{R_l + R} \left(1 + s \left[\frac{L}{R_l + R} + \left(R_l || R\right) C\right] + s^2 \left[\frac{R}{R_l + R}\right] LC\right)$$

(3). Using (60), the driving point input impedance is

$$Z_{in}(s) = \left(\frac{R_l + R}{\sqrt{L}}\right) + s \left(L + R_l RC\right) + s^2 RLC$$

$$= \left[\frac{1}{L + sR_l C + s^2 LC}\right]$$

(4). From (61) and recalling that $Z_s = 0$, the driving point output impedance is found to be

$$Z_{out}(s) = \frac{R + sL + s^2 RLC}{1 + sRC}$$

COMMENTS: It is notable that the chain parameter concept allows for the formulation of the foregoing gain and I/O impedance relationships without need of laborious circuit analysis. As a check on the propriety of the results, observe that as expected, the zero frequency voltage gain is the resistive divider, $(R_l/R_l + R)$, the zero frequency value of the driving point input impedance is $(R_l + R)$, and the zero frequency output impedance is simply $R$.

3.0. TWO PORT METHODS OF CIRCUIT ANALYSIS

The two port parameter sets introduced in the preceding section of material allow for an unambiguous volt-ampere characterization of any linear two port network in terms of the electrical properties that are observable and measurable at the input and output ports of the network. The equivalent circuits respectively corresponding to the hybrid h-, hybrid g-, short circuit y-, and open circuit z-parameters exploit superposition theory and comprise a modest extension of the classic one port formulation of the Thévenin and Norton theorems. These models are the fundamental tools that expedite a computationally efficient analysis of the transfer and driving point characteristics of terminated electrical and electronic systems whose intrinsic circuit topologies are either unknown or too complicated for straightforward circuit analyses predicated on the Kirchhoff laws.

3.1. CIRCUIT ANALYSIS IN TERMS OF h–PARAMETERS

Recalling Figure (9), the h-parameter equivalent circuit of the original, voltage-driven, terminated two port system in Figure (1) is the topology provided in Figure (28). Although either version of the system diagrammed in Figure (1) can be selected for analysis, the voltage-
driven version is chosen because the Thévenin nature of the h-parameter input port model is synergistic with the application of the Kirchhoff voltage law to said input port. In particular,

\[
V_s = (Z_s + h_{11})I_1 + h_{12}V_2,
\]

while at the output port,

\[
V_2 = -\frac{h_2I_1}{h_{22} + Y_l},
\]

where \(Y_l\) is the admittance corresponding to the terminating load impedance, \(Z_l\). If (74) is inserted into (73),

\[
\frac{V_s}{I_1} = Z_s + h_{11} - \frac{h_{12}h_{21}}{h_{22} + Y_l}.
\]

Equations (74) and (75) now yield a system voltage gain, \(A_v\), of

\[
A_v = \frac{V_2}{V_s} = \frac{-h_{21}}{1 - \frac{h_{12}h_{21}}{(h_{11} + Z_s)(h_{22} + Y_l)}}.
\]

### 3.1.1. Open Loop and Loop Gain Concepts

The rather cumbersome algebraic form of the voltage gain expression in (76) inspires neither analytical confidence nor relevant insights about the dynamic behavior of the system in Figure (28). A more illuminating format begins to materialize from the substitution,
\[ A_{vo} \triangleq -\frac{h_{21}}{(h_{11} + Z_s)(h_{22} + Y_l)}. \]  

(77)

whereupon (76) becomes

\[ A_v = \frac{V_2}{V_s} = \frac{A_{vo}}{1 + h_{12} A_{vo}}. \]  

(78)

Equation (78) implies

\[ V_2 = A_{vo} \left( V_s - h_{12} V_2 \right), \]  

(79)

which can be represented algebraically by the block diagram shown in Figure (29). This diagram underscores h-parameter \( h_{12} \) as the factor of the output voltage response that is fed back to the system input port. Since feedback is such a critically important phenomenon in virtually all electrical and electronic circuits and systems, the parameters implicit to the architecture in Figure (29) are worthy of further exploration.

\[ \text{Fig. (29). Block Diagram Model Of The Circuit In Figure (28). The Diagram Underscores The Feedback Inherent To The Subject Circuit.} \]

To begin this complementary exploration, note in Figure (29) that the signal path from the summing unit through the block labeled, \( A_{vo} \), and thence through the \( h_{12} \) block, constitutes a closed loop, which is doubtlessly the reason that the gain expression in (78) is traditionally termed the closed loop gain of the system undergoing study. Since setting \( h_{12} \) to zero reduces \( A_v \) in (78) to zero, and since \( h_{12} = 0 \) effectively opens the aforementioned closed loop, \( A_{vo} \), in (77) is logically termed the open loop gain. Note that the circuit in Figure (28) also verifies that \( A_v = A_{vo} \) when \( h_{12} = 0 \) since by inspection,

\[ I_1\bigg|_{h_{12}=0} = \frac{V_s}{Z_s + h_{11}}, \]  

(80)

whence by (74), the resultant gain is \( A_{vo} \), in accordance with (77).

The product, \( h_{12} A_{vo} \), appearing in the denominator on the right hand side of (78) is seen in Figure (29) as the multiplication of the open loop gain and the feedback factor. It is effectively the gain around the closed loop and is often termed the loop gain of the considered system. This h-parameter loop gain, say \( T_h(Z_s, Y_l) \), is functionally dependent on the source impedance, \( Z_s \), and the load admittance, \( Y_l \), and is defined by
\[ T_h(Z_s, Y_l) \equiv h_{12} A_{vo} = -\left( \frac{h_{12}}{h_{11} + Z_s} \right) \left( \frac{h_{21}}{h_{22} + Y_l} \right), \tag{81} \]

whence (78) is expressible as

\[ A_v = \frac{V_2}{V_s} = \frac{A_{vo}}{1 + T_h(Z_s, Y_l)}. \tag{82} \]

It is interesting to note that the second parenthesized factor on the right hand side of (81) is the negative ratio of the output port voltage, \( V_2 \), to the input port current, \( I_1 \), where \( V_2 \) and \( I_1 \) are recalled as the independent variables of \( h \)-parameter modeling. In other words, for an assumed input port current, \( I_1 \), the subject second factor is the negative forward transimpedance, \(-V_2/I_1\), as is suggested in Figure (30a). On the other hand, and as is portrayed by Figure (30b), the first factor comprising the loop gain in (81), inclusive of the negative sign, is the reverse transadmittance ratio, \( I_1/V_2 \), for the case of zero signal source excitation, \( V_s = 0 \). In other words, the negative first factor on the right hand side of (81) defines the input port current resulting exclusively from a presumed output port voltage. The loop gain concept is now apparent. In particular, the loop gain, which is always dimensionless, can be viewed conceptually as

![Diagram](a). Output Port Model Of The Equivalent Circuit In Figure (28), Which Is Used To Compute the Negative Input Port -To- Output Port Forward Transimpedance, \(-V_2/I_1\), Component Of The Circuit Loop Gain. (b). Input Port Model Of The Equivalent Circuit In Figure (28), Which Is Used To Compute the Output Port -To- Input Port Reverse Transadmittance, \( I_1/V_2 \), Component Of The Circuit Loop Gain Function, \( T_h(Z_s, Z_l) \).

\[ T_h(Z_s, Y_l) = -\left( \frac{h_{12}}{h_{11} + Z_s} \right) \left( \frac{h_{21}}{h_{22} + Y_l} \right) = \left( \frac{I_1}{V_2} \right) \left( \frac{V_s = 0}{-V_2} \right), \tag{83} \]
which is a product of two gains formed of the independent modeling variables. In particular, it is
product of the phase-inverted forward gain (transimpedance) from input port-to-output port and
the zero signal value of the reverse gain (transadmittance) from output port-to-input port.

The loop gain of a linear circuit or system is a critically important metric for several
reasons, two of which can be comprehended immediately. The first of these reasons derives
from the presumption that over a stipulated range of signal frequencies, the magnitude of the
loop gain is significantly larger than unity. Under this presumption, (81) and (82) combine to
deliver a closed loop, or actual, voltage gain of

\[ A_v = \frac{V_2}{V_s} = \frac{A_{vo}}{1 + T_h(Z_s', Y_l)} \approx \frac{I}{h_{12}}, \quad (84) \]

which is dependent on only the feedback h-parameter, \( h_{12} \), as opposed to a dependence on four h-
parameters, a source impedance, and a load admittance. To the extent that \( h_{12} \) can be physically
implemented as a network function that is dependent on a ratio of controllable passive compo-
nents, the achievable voltage gain is rendered reliable and analytically predictable. This laudable
attribute is particularly germane to integrated electronics whose active components are invariably
plagued by model parameters that are either ill-defined or poorly controlled during monolithic
processing. In other words, a sufficiently large loop gain magnitude delivers an actual gain that
is rendered relatively insensitive to both the h-parameters, \( h_{11}, h_{21}, \) and \( h_{22} \), and the source and
load terminations, \( Z_s \) and \( Y_l \), whose precise values are also somewhat unclear in broad varieties
of practical system applications. Note, however, that since closed loop gains larger than unity
are generally desirable, \( h_{12} \) is necessarily less than unity, which forces the open loop gain, \( A_{vo} \)
to be very large magnitude. Unfortunately, large open loop gains, such as those that prevail in
commercially available operational amplifiers, portend of potentially serious bandwidth limi-
tations. The upshot of the matter is that while large loop gains are assuredly advantageous in
active electronics from the perspective of gain desensitization with respect to parametric
uncertainties and tolerances, they are generally difficult to achieve in broadband systems.

A second reason underlying the importance of the loop gain is the picture that this metric
conveys with respect to the stability of active networks. In Figure (30b), consider the case in
which over a range of signal frequencies, the algebraic sign of \( h_{12}V_2 \) is such as to increase the
input port current, \( I_1 \). This so-called positive feedback would mean that feedback alone –
divorced of any source excitation– increases \( I_1 \), which results in an increase in the magnitude of
the output port voltage, \( V_2 \), which results in further increases in \( I_1 \), and so forth. In other words,
the circuit or system under investigation is potentially unstable and, pending the extent by which
\( I_1 \) increases, may be outright unstable. Although a definitive stability analysis\[5\] is a complicated
frequency domain task that is beyond the scope of the present discourse, a clue as to the loop
gain circumstances surrounding potential instability derives from an elementary consideration of
low frequencies, where all parameters and terminations are real numbers. Specifically, \( I_1 \)
increases and is therefore a positive current with \( V_s = 0 \) if \( h_{12}V_2 \) is negative. Because of (74),
\( h_{12}V_2 < 0 \) requires \( h_{12}h_{21}/(h_{22} + Y_l) > 0 \). Since (83) yields

\[ \frac{h_{12}h_{21}}{h_{22} + Y_l} = -\left(h_{11} + Z_s\right)T_h\left(Z_s', Y_l\right), \quad (85) \]
the undesirable instability situation requires that the loop gain, \( T_h(Z_s, Y_l) \), be negative, assuming the routine case of positive real impedances, \( h_{11} \) and positive \( Z_s \). In other words, a negative loop gain (at least at low signal frequencies) is tantamount to network potential instability. In contrast, positive loop gain assures network stability. Since positive loop gain requires \( h_{12}V_2 > 0 \), input current \( I_1 \) decreases, the output response remains forever bounded for bounded inputs, and the system under consideration is said to be characterized by negative feedback.

The phrase, potential instability, is used in the foregoing paragraph in the context of stipulating \( T_h(Z_s, Y_l) < 0 \) as a necessary, but not sufficient, condition for circuit instability. For example, if the loop gain is negative, but has a magnitude less than unity, the circuit remains stable. If on the other hand, the loop gain is negative with a magnitude exceeding one, there must exist at least one frequency where the loop gain is precisely negative one. At these frequencies, the considered circuit is unstable in the sense that its gain is boundless, which means that output voltages are established even when the signal source is nulled. If \( T_h(Z_s, Y_l) = -1 \) at precisely one value of frequency, say \( \omega_0 \), the circuit is technically unstable but nonetheless useful in communications and other systems as a sinusoidal oscillator whose steady state radial frequency of oscillation is \( \omega_0 \)[6].

### 3.1.2 I/O Impedances

The loop gain is also instrumental with respect to stipulating the magnitude and general nature of network impedances established at input and output ports. To this end, consider Figure (31a), which relies on the model in Figure (28) to delineate the equivalent circuit pertinent to a determination of the driving point input impedance, \( Z_{in} \). A straightforward circuit analysis readily confirms,

![Equivalent Circuit For The Evaluation Of The Driving Point Input Impedance, \( Z_{in} \), Of The Circuit Modeled In Figure (28).](image)

![Equivalent Circuit For Calculating The Driving Point Output Admittance Of The Circuit Of Figure (28).](image)
\[
Z_{in} = \frac{V_x}{I_x} = h_{11} - \frac{h_{12}h_{21}}{h_{22} + Y_l} = h_{11}\left[1 - \frac{h_{12}h_{21}}{h_{11}(h_{22} + Y_l)}\right],
\]  
(86)

where \(I_x\) is a test independent input port current, \(V_x\) is the input port response to this current, and \(V_x/I_x\) exploits Ohm’s law to determine the input impedance. Observe an input impedance of \(h_{11}\) in the absence of feedback \((h_{12} = 0)\), which means that \(h_{11}\) can be thought of as an open loop input impedance. Moreover, (83) allows (86) to be expressed as

\[
Z_{in} = h_{11} - \frac{h_{12}h_{21}}{h_{22} + Y_l} = h_{11}\left[I + T_h\left(0, Y_l\right)\right],
\]  
(87)

where \(T_h(0, Y_l)\) symbolizes the h-parameter loop gain under the condition of zero source impedance \((Z_s = 0)\). Since the loop gain is proportional to the open loop gain, and since the magnitude of the open loop voltage gain for zero source impedance is surely larger than it is for nonzero source impedance, \(|T_h(0, Y_l)| > |T_h(Z_s, Y_l)|\), which confirms

\[
Z_{in} = h_{11}\left[I + T_h\left(0, Y_l\right)\right] > h_{11}\left[I + T_h\left(Z_s, Y_l\right)\right].
\]  
(88)

And since the magnitude of the loop gain is desirably large for acceptable gain desensitization with respect to parametric vagaries, the last result indicates that the system in Figure (28) is capable of a driving point input impedance that is significantly larger than the h-parameter prediction of its counterpart open loop value.

Because of the Norton nature of the h-parameter output port, the driving point output admittance, \(Y_{out}\), is more conveniently evaluated than is the corresponding output impedance. Figure (31b) can be used to demonstrate that

\[
Y_{out} = \frac{I_y}{V_y} = h_{22} - \frac{h_{12}h_{21}}{h_{11} + Z_s} = h_{22}\left[I + T_h\left(Z_s, 0\right)\right],
\]  
(89)

where (83) has been used once again, and \(T_h(Z_s, 0)\) is the \(Y_l = 0\) value of the h-parameter loop gain. Comments analogous to those made in regard to the input impedance can be proffered for the output admittance. In particular, (89) shows that the driving point output impedance can be considerably larger than its open loop value, which is \(h_{22}\). It follows that the closed loop output impedance can be substantively smaller than the open loop output impedance predicted by h-parameters.

**EXAMPLE #6:**

Figure (32) is an extension of the model given in Figure (12) in that it addresses an emitter-degenerated bipolar transistor amplifier whose input and output ports are terminated. The signal source applied to the amplifier input port has a Thévenin resistance, \(R_s\), of 75 \(\Omega\), while the amplifier output port drives a resistive load, \(R_l\), of 3

\[K\Omega.\]  
Recall that the amplifier parameters are \(r_i = 2.2 K\Omega, r_o = 25 K\Omega, \beta = 90,\) and \(R_e = 80 \Omega.\) The results of Example #1 are the h-parameters, \(h_{11} = 9.46 K\Omega, h_{21} = 89.71\) 
amps/amp, \(h_{12} = 3.19 mV/V,\) and \(h_{22} = 39.87 \mu S.\) Determine the open loop voltage
gain, $A_{vo}$, of the amplifier, the loop gain, $T_h(R_s, G_l)$, the closed loop gain, $A_v$, the driving point input resistance, $R_{in}$, and the driving point output resistance, $R_{out}$.

![Small Signal Equivalent Circuit Of The Emitter-Degenerated Common Emitter Amplifier Considered In Example #6. The Model And Circuit Parameters Are $r_i = 2.2 \, K\Omega$, $r_o = 25 \, K\Omega$, $\beta = 90$, $R_e = 80 \, \Omega$, $R_s = 75 \, \Omega$, and $R_l = 3 \, K\Omega$.](image)

**SOLUTION:**

(1). Using (77) with $Z_s = R_s = 75 \, \Omega$ and $Y_l = 1/R_l = 1/3 \, K\Omega$, the open loop voltage gain of the subject amplifier is found to be $A_{vo} = -25.21$, or a magnitude of 28.03 dB. From (81), the loop gain is $T_h(R_s, G_l) = -80.42(10^{-3})$, which is only $-21.89$ dB. It follows from (78) that the closed loop, or actual, voltage gain is $A_v = -27.42$, or a closed loop gain magnitude of 28.76 dB.

(2). The $R_s = 0$ value of the loop gain is, by (83), $T_h(0, G_l) = -81.06(10^{-3})$, while the $G_l = 0$ value of this metric is $T_h(R_s, 0) = -752.77(10^{-3})$. Using (88) and (89), the driving point input resistance is calculated to be $R_{in} = 8.69 \, K\Omega$, while, the driving point output conductance is $G_{out} = 9.86 \, \mu S$, whence an output resistance of $R_{out} = 101.45 \, K\Omega$.

**COMMENTS:** The single stage emitter-degenerated bipolar amplifier is so ubiquitous in state of the art electronics that rarely is it perceived as a positive feedback architecture. Yet, the loop gain, as calculated above, is a negative number but fortunately, it is a negative number whose magnitude is considerably less than one. Indeed, this loop gain magnitude is so much smaller than one that it is often tacitly ignored in gain and input impedance calculations, which probably explains why its positive feedback nature is typically unnoticed. But because of this small loop gain, the amplifier at hand is a terrible voltage signal processor, principally because its extremely high output impedance renders the closed loop voltage gain vulnerable to even modest load termination uncertainties.

### 3.2. CIRCUIT ANALYSIS IN TERMS OF g–PARAMETERS

The circuit analyses executed in terms of a g-parameter model of a linear two port network are similar to those conducted in conjunction with h-parameters, and indeed, with y- and z-parameters. In the case of g-parameters, the model in Figure (14) allows the system of Figure (1) to be represented by the equivalent circuit offered in Figure (33). The shunt nature of the g-parameter model input port renders a Norton representation of the signal source more expedient.
than a Thévenin architecture. Moreover, the series nature of the g-parameter output port model encourages a view of the load termination as an impedance, as opposed to an admittance.

![Linear Two Port Network Diagram]

Fig. (33). The g-Parameter Equivalent Circuit Of The Linear Two Port Network In Figure (1). The Current-Driven Version Of Figure (1) Is Chosen Because Of The Norton Nature Of The g-Parameter Model Input Port.

A conventional circuit analysis of the equivalent circuit in Figure (33) yields a current gain, $A_i$, of

$$A_i = \frac{I_2}{I_s} = \frac{g_{21}}{\left(g_{11} + g_{22} + Z_l\right)} \frac{g_{21}}{\left(g_{11} + Y_s\right)} \frac{g_{21}}{g_{22} + Z_l},$$

(90)

which is expressible as

$$A_i = \frac{I_2}{I_s} = \frac{A_{io}}{1 + T_g \left(Y_s, Z_l\right)}.$$  \hspace{1cm} (91)

In the last expression

$$A_{io} = -\frac{g_{21}}{\left(g_{11} + g_{22} + Z_l\right)}$$

(92)

is the open loop current gain; that is, it is the current gain of the two port system in Figure (1) under the condition that the feedback g-parameter, $g_{12}$, is nulled. Moreover,

$$T_g \left(Y_s, Z_l\right) \triangleq g_{12} A_{io} = -\left(\frac{g_{12}}{g_{11} + Y_s}\right) \frac{g_{21}}{g_{22} + Z_l}$$

(93)

is the g-parameter loop gain of the two port network. Note that this loop gain is expressed as an explicit function of the Thévenin source admittance, $Y_s$, and the terminating load impedance, $Z_l$. 
Moreover, observe the striking similarity in form of (90) -through- (93) with their respective h-parameter counterpart relationships.

The aforementioned functional similarity with corresponding h-parameter expressions applies equally well insofar as the driving point input admittance, $Y_{in}$, and the driving point output impedance, $Z_{out}$, in Figure (33) are concerned. Specifically, it can be demonstrated that

$$Y_{in} = g_{11} - \frac{g_{12}g_{21}}{g_{22} + Z_l} = g_{11} \left[ l + T_g \left( 0, Z_l \right) \right]. \tag{94}$$

and

$$Z_{out} = g_{22} - \frac{g_{12}g_{21}}{g_{11} + Y_s} = g_{22} \left[ l + T_g \left( Y_s, 0 \right) \right]. \tag{95}$$

In (94), the source admittance (not the source impedance) is nulled in the course of evaluating the input admittance. In (95), the load impedance (not the load admittance) is set to zero for the output impedance computation.

### 3.3. CIRCUIT ANALYSIS IN TERMS OF y–PARAMETERS

If the two port system of Figure (1) is modeled by short circuit admittance, or $y$-, parameters, the model in Figure (18) applies, and the equivalent circuit in Figure (34) results. The shunt nature of the $y$-parameter model input port suggests the prudence of a Norton representation of the signal source, while the similar Norton topology of the $y$-parameter output port directs an admittance representation of the load admittance. With port voltage $V_2$ as the independent output variable and Norton signal current $I_s$ as the known independent energy source, the closed loop gain is a transimpedance, $Z_f$, which can be shown to be
\[
Z_f = \frac{V_2}{I_s} = \frac{Z_{fo}}{1 + T_y(Y_s, Y_l)},
\]

(96)

where

\[
T_y(Y_s, Y_l) = y_{12}Z_{fo} = -\left(\frac{y_{12}}{y_{11} + Y_s}\right)\left(\frac{y_{21}}{y_{22} + Y_l}\right)
\]

(97)
is the loop gain expressed in terms of y-parameters, and

\[
Z_{fo} = -\frac{y_{21}}{(y_{11} + Y_s)(y_{22} + Y_l)}
\]

(98)
is the open loop gain; that is, the closed loop gain value under the condition of \(y_{12} = 0\). A conventional Ohm’s law type of circuit analysis confirms driving point input and output admittances, \(Y_{in}\) and \(Y_{out}\), respectively, of

\[
Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_l} = y_{11}\left[1 + T_y(0, Y_l)\right]
\]

(99)

and

\[
Y_{out} = y_{22} - \frac{y_{12}y_{21}}{y_{11} + Y_s} = y_{22}\left[1 + T_y(Y_s, 0)\right].
\]

(100)

### 3.4. CIRCUIT ANALYSIS IN TERMS OF Z–PARAMETERS

The open circuit impedance, or z-, parameter model of a linear two port network is shown in Figure (23). The use of this model in conjunction with the system of Figure (1) delivers the equivalent circuit in Figure (35). The series nature of both the input and output ports of this equivalent circuit encourages an impedance characterization of the load termination and a Thévenin representation of the applied signal source. Accordingly, the most expediently evaluated forward gain is the transadmittance, \(I_2/V_s\), where \(I_2\) is the output port current and, of course, \(V_s\) is the Thévenin signal voltage.

A traditional analysis of the model in Figure (35) delineates the aforementioned transadmittance as

\[
Y_f = \frac{I_2}{V_s} = \frac{Y_{fo}}{1 + T_z(Z_s, Z_l)},
\]

(101)

where

\[
Y_{fo} = -\frac{z_{21}}{(z_{11} + Z_s)(z_{22} + Z_l)}
\]

(102)
is the open loop transadmittance value for the zero feedback condition, $z_{12} = 0$. Moreover

$$T_z(Z_s, Z_1) = z_{12} Y_{fo} = -\left(\frac{z_{12}}{z_{11} + Z_s}\right)\left(\frac{z_{21}}{z_{22} + Z_1}\right)$$

(103)

is the $z$-parameter prediction of the system loop gain. The indicated input and output impedances, $Z_{in}$ and $Z_{out}$, respectively, can be shown to be

$$Z_{in} = z_{11} - \frac{z_{12}z_{21}}{z_{22} + Z_1} = z_{11}\left[1 + T_z(0, Z_1)\right]$$

(104)

and

$$Z_{out} = z_{22} - \frac{z_{12}z_{21}}{z_{11} + Z_s} = z_{22}\left[1 + T_z(Z_s, 0)\right].$$

(105)

EXAMPLE #7:

The equivalent circuit given in Figure (36) is an approximate, low frequency, common source, model of a MOSFET amplifier that can be designed to realize match terminated impedance characteristics. With reference to the diagram in Figure (36), “match termination” means that for a Thévenin source resistance, $R_s$, equal to the terminating load resistance, $R_l$, the driving point input resistance, $R_{in}$, and the driving point output resistance, $R_{out}$, are equal and, in fact, are equal to $R_s$. In other words, if $R$ symbolizes the numerical value of the source and load resistances, $R_s = R_{in} = R_{out} = R_l \equiv R$ under match terminated operating conditions. Use two port parameter techniques to determine the values of the circuit resistances, $R_s$ and $R_l$, commensurate with a match terminated condition. For this situation, derive an expression for the resultant voltage gain, $A_v = V_2/V_s$. For the purpose of this problem, assume that the resistance, $R_s$, which represents the static resistance seen between the gate and source
terminals of the utilized MOSFET, is very large. No presumption should be made about the degeneration resistance, $R_g$, in the source terminal of the MOSFET circuit model.

![Diagram of a two-port network](image)

**Fig. (36).** The Low Frequency, Small Signal Equivalent Circuit Of The Match Terminated Amplifier Considered In Example #7.

**SOLUTION:**

1. The first step in the solution procedure is a determination of the appropriate two port parameters of the network that couples the signal source to the load termination in Figure (36). The short circuit admittance parameters are somewhat arbitrarily selected herewith and to this end, Figure (37a), which depicts the subject network under the condition of a short circuited output port, is pertinent to the evaluation of the $y$-parameters, $y_{11}$ and $y_{21}$. Note in this figure that the current conducted by resistance $R_g$ is

![Diagram of circuit model](image)

**Fig. (37).** (a). Circuit Model Used To Evaluate The $y$-Parameters, $y_{11}$ and $y_{21}$, in Example #7. (b). Equivalent Circuit For Calculating The $y$-Parameters, $y_{12}$ and $y_{22}$, in Example #7.

\[
\frac{V}{R_i} + g_m V = \frac{V}{R_i} \left( 1 + g_m R_i \right)\\
\]

whence the input port voltage, $V_i$, is expressible as

\[
V_i = \frac{V}{R_i} \left[ R_i + \left( 1 + g_m R_i \right) R_g \right].
\]

In Figure (37a), it follows that
\[ I_1 = \frac{V}{R_i} + \frac{V_1}{R_f}, \]
from which
\[ y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0} = \frac{I}{R_f} + \frac{I}{R_i + (1 + g_m R_i) R_g} = \frac{I}{R_f}. \]
Moreover, since
\[ I_2 = g_m V - \frac{V_1}{R_f}, \]
the short circuit forward transadmittance, \( y_{21} \), is
\[ y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0} = \frac{g_m R_i}{R_i + (1 + g_m R_i) R_g} \approx \frac{g_m - 1}{R_f}, \]
where
\[ g_{me} = \frac{g_m}{1 + g_m R_g} \]
represents an effective forward transconductance. Note that the impact of the source terminal degeneration resistance, \( R_g \), is a degradation of the original value of the MOSFET forward transconductance, \( g_m \).

(2). Figure (37b), offers the equivalent circuit appropriate to the computation of the \( y \)-parameters, \( y_{12} \) and \( y_{22} \). In this figure that the current conducted by resistance \( R_g \), is identical to the current flowing through \( R_g \) in Figure (37a). Hence, the input port voltage, \( V_i \), has the same algebraic expression for both circuit models, which means that with \( V_i = 0 \), voltage \( V \) is also zero. It follows immediately that
\[ y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0} = -\frac{I}{R_f} \]
and
\[ y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0} = \frac{I}{R_f} + \frac{I}{R_x}. \]

(3). If the Thévenin source impedance and the terminating load impedance are purely resistive and each equal to the stipulated value, \( R, Y_s = Y_l = 1/R \) in (99) and (100). A further inspection of these two relationships indicates that the driving point input admittance, \( Y_{in} \) (conductance in this case), and the driving point output admittance, \( Y_{out} \) (also presently a conductance), are equal to one another for \( Y_i = Y_l = 1/R \) if and only if \( y_{11} = y_{22} \). Using the results of the preceding two computational steps, \( y_{11} = y_{22} \) if the shunting output port resistance, \( R_x \), is chosen to satisfy
\[ R_x = R_g + \left( 1 + g_m R_g \right) R_i, \]
which, for large \( R_i \), reduces to...
\[ R_x \approx \left( 1 + g_m R_g \right) R_i. \]

Note, therefore that large \( R_i \) commands a proportionately large \( R_x \).

(4). Returning to either (99) or (100),

\[ \frac{l}{R} = y_{11} - \frac{y_{12}y_{21}}{y_{11} + \frac{l}{R}}. \]

Using the y-parameter results of Steps #1 and #2 and the result for \( R_x \) in Step #3, this requirement can be shown to imply

\[ R_f = \frac{\left( 2 + g_m R_x \right) R_x}{\left( R_x/R \right)^2 - l}. \]

Since \( R_x \) is very large by virtue of its direct proportionality to the very large model resistance, \( R_i \),

\[ R_f = g_m R_x^2 = \frac{g_m R_x^2}{1 + g_m R_g}. \]

(5). The transimpedance of the network in Figure (36) is given by (96) -through- (98). Transimpedance \( Z_f \) relates to the network voltage gain, \( A_v \), in accordance with

\[ A_v = \frac{V_2}{V_s} = \frac{V_2}{I_s R} = \frac{Z_f}{R}, \]

where the source resistance, \( R_s \), is equated to its match terminated value of \( R \). With \( y_{11} = y_{22} \) and \( Y_s = Y_l = R_s = R \), the preceding result and the aforementioned gain equations produce

\[ A_v = \frac{V_2}{V_s} = -\frac{y_{21}/R}{\left( y_{11} + \frac{l}{R} \right)^2 - y_{12}y_{21}}. \]

The substitution of the pertinent computational results of Steps #1-#4 into this expression, followed by a bit of algebraic acrobatics, yields

\[ A_v = \frac{V_2}{V_s} \approx -\frac{g_m R - 1}{2}. \]

COMMENTS: Match terminated amplifiers are pivotal to state of the art communication circuits. These circuits are plagued by signal strength levels that are comparable to electrical noise floors, thereby rendering reliable signal detection problematic. Matched terminations at a given port assure maximum power transfer therein, which ensures minimal, if any, signal power loss between the effective source and load of this port. Although the traditional engineering design approaches that underpin the realization of a match terminated amplifier can prove to be a cumbersome undertaking, this example points out the relevant propriety of two port parameters. In particular, the two port parameters, and particularly the y-parameters exploited herein, support the design objective by highlighting the
fundamental requirements supportive of, and streamlining the design-oriented computation steps that result in, match terminated circuit operation.

4.0. SYSTEMS OF INTERCONNECTED TWO PORTS

The closed loop gain (voltage gain, current gain, transimpedance, or transadmittance) of a linear two port network is nominally independent of the source and load terminations and nominally inversely dependent on the two port feedback parameter \((h_{12}, g_{12}, y_{12}, \text{ or } z_{12})\) if the magnitude of the network loop gain is sufficiently large. For most active networks divorced of purposefully applied external feedback and almost all passive circuits, the internal feedback parameter is too small to deliver the loop gain magnitude required for this parametric desensitization.

To ensure reliable and predictable closed loop performance, the internal feedback parameter of an active two port network is commonly augmented by incorporating a second feedback network extrinsic to the active cell. This appended feedback loop is routinely, but not universally, formed of passive components for at least two reasons. First, the values of passive elements, and especially the ratios of passive element component values, are more predictable than are the parameters of active devices. Thus, to the extent that the incorporated external feedback network is the dominant vehicle for determining the effective feedback parameter of the overall closed loop system, the resultant closed loop gain becomes a predictable system performance metric. A second reason underpinning the use of passive external feedback structures stems from the fact that passive circuits are reciprocal architectures that are incapable of providing gain. They are thus stable structures that do not substantially alter the forward gain magnitude and phase characteristics of the active cells with which they interact. In particular, the magnitude of the forward transmission parameter of a passive feedback cell is likely to be significantly smaller than the magnitude of the corresponding forward transmission parameter of the active cell to which it is interconnected.

When the appended feedback loop is connected from the output port of the original open loop two port network to its input port, the nature of the feedback is said to be global. There are four commonly exploited forms of global feedback: series-shunt feedback, shunt-series feedback, shunt-shunt feedback, and series-series feedback. Assuming that the two port parameters of the original open loop structure and those of the appended feedback subcircuit are unaltered by their input and output port electrical interconnections, the analysis of the resultant global architecture can be straightforwardly formulated in terms of a mere superposition of their appropriate respective two port parameters \([7]\). That which constitutes “appropriate” two port parameters in the analysis of global feedback systems is largely a matter of technical common sense, as the following subsections illustrate.

4.1. SERIES-SHUNT FEEDBACK

Series-shunt feedback materializes by interconnecting two networks in such a way as to ensure the satisfaction of two operational constraints. The first of these constraints is that the overall input port voltage of the global interconnection is the sum of the input port voltages of the individual two networks. Second, the net output port current is precisely the sum of the respective output port currents for the two interconnected structures. The situation at hand is abstracted in Figure (38a), which shows an “uncompensated” linear two port network, Network
A, that is “compensated” by a second linear two port network, Network B, that interconnects with the first network as a series-shunt feedback structure. The series nature of the interconnected input ports of these two networks is confirmed by the observation that the net input port voltage, $V_1$, relates to the input port voltage, $V_{1a}$, of Network A and the input port voltage, $V_{1b}$, of Network B in accordance with

\[
I_{1b} = k_h I_{1a}
\]

Moreover, the net output port current, $I_2$, conducted by the extrinsic load impedance, $Z_l$, is seen to be the sum of the output currents, $I_{2a}$ and $I_{2b}$, of Networks A and B, respectively; that is,

\[
I_2 = I_{2a} + I_{2b}
\]

The shunt interconnection nature of the two network output ports is further confirmed by the observation that the overall output port voltage, $V_2$, is identical to the output port voltage $V_{2a}$, of Network A and the output port voltage, $V_{2b}$, of Network B. Specifically,

\[
V_2 = V_{2a} = V_{2b}
\]

Although a strictly series input port architecture mandates that the net input current, $I_1$, is identical to both of the individual input port currents, $I_{1a}$ and $I_{1b}$, such current equality cannot generally

\[
V_1 = V_{1a} + V_{1b}
\]

\[
I_2 = I_{2a} + I_{2b}
\]

\[
V_2 = V_{2a} = V_{2b}
\]
be guaranteed, particularly when Network $A$ is an active configuration. However, the linearity of the interconnected closed loop system allows the conjecture that the Network $B$ input port current, $I_{lb}$, is proportional to $I_{la}$, the input port current of Network $A$. Accordingly, let

$$I_{lb} = k_h I_{la},$$  \hspace{1cm} (109)

where $k_h$ is a constant, independent of all network voltages and currents, determined by the electrical properties of Network $A$.

Because the h-parameter equivalent circuit is effectively a series-shunt topology evoking input port voltage $V_1$ and output port current $I_2$, both of which are sums of respective port variables as per (106) and (107), as dependent variables, h-parameters are used to model each of the two subsystems in Figure (38a). Accordingly,

$$\begin{bmatrix} V_{1a} \\ I_{2a} \end{bmatrix} = \begin{bmatrix} h_{11a} & h_{12a} \\ h_{21a} & h_{22a} \end{bmatrix} \begin{bmatrix} I_{1a} \\ V_{2a} \end{bmatrix} = \begin{bmatrix} h_{11a} & h_{12a} \\ h_{21a} & h_{22a} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix},$$  \hspace{1cm} (110)

where (108) and the fact that $I_{la}$ is the overall input port current, $I_1$, are exploited. For Network $B$,

$$\begin{bmatrix} V_{1b} \\ I_{2b} \end{bmatrix} = \begin{bmatrix} h_{11b} & h_{12b} \\ h_{21b} & h_{22b} \end{bmatrix} \begin{bmatrix} I_{lb} \\ V_{2b} \end{bmatrix} = \begin{bmatrix} h_{11b} & h_{12b} \\ h_{21b} & h_{22b} \end{bmatrix} \begin{bmatrix} k_h I_{la} \\ V_2 \end{bmatrix} = \begin{bmatrix} k_h h_{11b} & h_{12b} \\ k_h h_{21b} & h_{22b} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix},$$  \hspace{1cm} (111)

where (108), (109), and the rules of matrix algebra, have been applied. Noting that the input port current, $I_1$, and the output port voltage, $V_2$, appear as common independent variables in both of the preceding two relationships, (106) and (107) combine with (110) and (111) to deliver

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \left(h_{11a} + k_h h_{11b}\right) & \left(h_{12a} + h_{12b}\right) \\ \left(h_{21a} + k_h h_{21b}\right) & \left(h_{22a} + h_{22b}\right) \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}. \hspace{1cm} (112)$$

This elegantly simple result conduces a straightforward delineation of the h-parameter equivalent circuit for the series-shunt feedback network of Figure (38a). This model appears in Figure (38b), where from (112), it is understood that the effective h-parameters of the overall feedback system are

$$h_{11e} = h_{11a} + k_h h_{11b},$$  
$$h_{12e} = h_{12a} + h_{12b},$$  
$$h_{21e} = h_{21a} + k_h h_{21b},$$  
$$h_{22e} = h_{22a} + h_{22b}, \hspace{1cm} (113)$$

The performance metrics of the series-shunt feedback structure now derive directly from the pertinent equations given in Section (3.1), subject to the proviso therein that, $h_{ij}$ is replaced by the effective parameter, $h_{ije}$.
EXAMPLE #8:

Figure (39a) is a classic example of series-shunt feedback implemented in bipolar junction transistor (BJT) technology. As is suggested in this figure, active Network A is the two stage transistor amplifier, while feedback Network B is the voltage divider comprised of the resistances, $R_1$ and $R_2$. Assume that both transistors are identical and are biased identically (biasing is not shown) and that Figure (38b) is a sufficiently accurate low frequency model of each transistor. In this model, take $r_i = 2 \, K\Omega$ and $\beta = 120$. Additionally, let $R_f = 150 \, \Omega$, and $R_s = 900 \, \Omega$. Assume that the signal source resistance, $R_s$, is 75 $\Omega$, while the terminating load resistance, $R_l$, is 1.2 $K\Omega$. Calculate the overall voltage gain, $A_v = V_2/V_s$, the driving point input resistance, $R_{in}$, and the driving point output resistance, $R_{out}$. Additionally, deduce appropriately simplified analytical relationships for each of these three performance indices.

\[ V_1a = I_1 R_1 + V_2 \]
\[ V_2 = I_2 R_l \]
\[ I_1 = \beta I_2 \]

**Fig. (39).** (a). Series-Shunt Feedback Amplifier Realized in Bipolar Junction Transistor (BJT) Technology. (b). Simplified Small Signal, Low Frequency Model Of A BJT.

**SOLUTION:**

(1). The equivalent circuit of the overall feedback configuration is depicted in Figure (40a), where use has been made of the bipolar model suggested in Figure (39b). Since feedback Network B is connected in series-shunt with active Network A, h-parameters are the appropriate modeling vehicle for Network B. To this end,
Fig. (40). (a). Small Signal, Low Frequency Equivalent Circuit Of The Feedback Amplifier In Figure (39a). (b). The h-Parameter Model Of Feedback Network B. (c). Simplified Version Of The Equivalent Circuit In (a). Note That The Topology Of This Architecture Reflects That Of The Classic h-Parameter Equivalent Circuit Of A Linear Network.
This result establishes Figure (40b) as the h-parameter equivalent circuit of feedback Network B. If the feedback network in the amplifier of Figure (40a) is replaced by its h-parameter model of Figure (40b), the equivalent circuit of the overall amplifier can be configured as illustrated in Figure (40c). In the latter diagram, use is made of the fact that current $I$ in Figure (40a) is $-\beta I_{1a} = -\beta I_1$, whence $\beta I$ in the same figure becomes $-\beta^2 I_1$. Moreover, observe that the input current, $I_{1b}$, of feedback Network B is $(\beta+1)I_{1a} = (\beta+1)I_1$, which implies that the constant, $k_{B}$, introduced in (109) is $k_B = (\beta+1)$. It follows that $h_{21b} I_{1b} = (\beta+1) h_{21b} I_1$.

(2). By comparing the model developed in Figure (40c) with the generalized h-parameter equivalent circuit in Figure (28), the hybrid h-parameters of the overall feedback amplifier can be deduced by mere inspection. In particular,

$$h_{11e} = r_i + (\beta + 1) \left( \frac{R_1}{R_2} \right) = 17.56 \, \text{K} \, \Omega,$$

$$h_{21e} = - \left[ \beta^2 + (\beta + 1) \frac{R_1}{R_1 + R_2} \right] = -14.42 \, \text{KA/} \, \text{A},$$

$$h_{12e} = \frac{R_1}{R_1 + R_2} = 1/7 \, \text{V/V},$$

$$h_{22e} = \frac{1}{R_1 + R_2} = 952.4 \, \mu \text{S}.$$

(3). The closed loop performance of the subject amplifier can now be determined directly from pertinent relationships in Section (3.1). From (77), the open loop voltage gain is $A_o = 457.9 = 53.22 \, \text{dB}$, and from (78), the corresponding closed loop voltage gain is $A_v = 6.90 = 16.77 \, \text{dB}$. Note a loop gain of $T_h(R_s, G_l) = 65.41 = 38.31 \, \text{dB}$.

(4). Using (87), the closed loop input resistance is $R_{in} = 1.17 \, \text{Meg} \, \Omega$, while (89) yields a closed loop output conductance of $G_{out} = 117.8 \, \text{mS}$, which equates to an output resistance of $R_{out} = 8.49 \, \Omega$.

(5). Since the loop gain in this example is very large, several simplified analytical relationships can be forged. Recalling (78) once again, the closed loop gain is approximately
\[ A_v = \frac{l_{12e}}{h_{12e}} = 1 + \frac{R_2}{R_1} = 7.0, \]

which is only 1.45\% higher than the precisely computed voltage gain.

(6). Because of large loop gain, the driving point input resistance, \( R_{in} \), is expressible as

\[ R_{in} = h_{11e} T_h(0, G_1), \]

which for large \( \beta \) is equivalent to

\[ R_{in} \approx \beta^2 R_i \left( \frac{R_1}{R_1 + R_1 + R_2} \right) = 1.15 \text{ Meg } \Omega. \]

This result is lower than that computed in Step #4 by only 1.54\%. Similarly, the output conductance, \( G_{out} = 1/R_{out} \), is

\[ G_{out} = h_{22e} T_h(R_s, 0), \]

or

\[ R_{out} \approx \frac{R_2}{\beta} = 7.5 \text{ } \Omega. \]

When compared to the calculation in Step #4, this result is seen to be in error by –11.7\%.

COMMENTS: Very large input resistance and very small output resistance combine to make the series-shunt feedback amplifier an excellent voltage amplifier. In particular, its low output resistance allows small load resistances to be driven without rendering the voltage gain significantly dependent on actual load resistance. Similarly, its large input resistance effectively desensitizes the voltage gain to uncertainties in source resistances. Best of all, the resultant approximate voltage gain is dependent on a resistance ratio, which is relatively easy to control accurately during monolithic processing. It is important to underscore the fact that these design-oriented observations derive directly from the fruits of a straightforward two port parameter analysis of the subject feedback configuration. In the absence of this two port methodology, a conventional circuit analysis of the amplifier at hand would likely have generated the documented numerical results without the insights that implicitly underpin innovative circuit design.

4.2. SHUNT-SERIES FEEDBACK

The shunt-series feedback amplifier, whose system level diagram is abstracted in Figure (41a) is exceptionally well-suited for current amplification because of the low input impedance and high output impedance it delivers. Accordingly, the signal source is represented as a Norton structure, and it is understood that the relevant output response variable of interest is the overall output port current, \( I_2 \). The shunt nature of the respective input port connections is underscored by the fact that the overall input port voltage, \( V_1 \), the input port voltage, \( V_{Ia} \), of Network \( A \) (which is generally the active unit of the feedback system), and the input port voltage, \( V_{Ib} \), of Network \( B \) are identical. Moreover, the overall input port current, \( I_1 \), is the sum of currents \( I_{1a} \) and \( I_{1b} \).
and $I_{1b}$, which respectively symbolize the currents flowing into the input ports of Networks $A$ and $B$. On the other hand, the overall output port voltage, $V_2$, is the sum of the output port voltage, $V_{2a}$, of Network $A$ and $V_{2b}$, the voltage developed across the output port of Network $B$. Although this output port voltage relationship suggests a series topology, the current, $I_{2b}$, conducted by the output port of Network $B$ is not necessarily the same as the output port current, $I_{2a}$, of Network $A$ because of electrical constraints implicit to the circuit architecture of Network $A$. However, system linearity compels that $I_{2b}$ be proportional to $I_{2a}$ and to this end, a proportionality constant, $k_{g}$, is introduced, as is indicated in Figure (41a).

![Figures (41a) and (41b)](image)

**Fig. (41).** (a) Shunt-Series Feedback Interconnection Of Two Linear Two Port Networks. (b) The g-Parameter Equivalent Circuit Of The Network In (a).

Because the g-parameter equivalent circuit is a shunt-series topology, g-parameters can be gainfully exploited to effect an efficient analysis of the shunt-series feedback amplifier. For Network $A$,

$$
\begin{bmatrix}
I_{1a} \\
V_{2a}
\end{bmatrix} =
\begin{bmatrix}
g_{11a} & g_{12a} \\
g_{21a} & g_{22a}
\end{bmatrix}
\begin{bmatrix}
V_{1a} \\
I_{2a}
\end{bmatrix} =
\begin{bmatrix}
g_{11a} & g_{12a} \\
g_{21a} & g_{22a}
\end{bmatrix}
\begin{bmatrix}
V_{1} \\
I_{2}
\end{bmatrix},
$$

(114)

and for Network $B$,

$$
\begin{bmatrix}
I_{1b} \\
V_{2b}
\end{bmatrix} =
\begin{bmatrix}
g_{11b} & g_{12b} \\
g_{21b} & g_{22b}
\end{bmatrix}
\begin{bmatrix}
V_{1b} \\
I_{2b}
\end{bmatrix} =
\begin{bmatrix}
g_{11b} & g_{12b} \\
g_{21b} & g_{22b}
\end{bmatrix}
\begin{bmatrix}
V_{1} \\
I_{2}
\end{bmatrix} =
\begin{bmatrix}
g_{11b} & k_{g} g_{12b} \\
g_{21b} & k_{g} g_{22b}
\end{bmatrix}
\begin{bmatrix}
V_{1} \\
I_{2}
\end{bmatrix}.
$$

(115)

Since $I_1 = I_{1a} + I_{1b}$ and $V_2 = V_{2a} + V_{2b}$, it follows that
\[
\begin{bmatrix}
I_1 \\
V_2
\end{bmatrix}
= \begin{bmatrix}
g_{11a} + g_{11b} \\
g_{21a} + g_{21b}
g_{12a} + k_g g_{12b} \\
g_{22a} + k_g g_{22b}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
I_s
\end{bmatrix},
\]
whence the effective g-parameters in the g-parameter equivalent circuit shown in Figure (41b) are
\[
g_{11e} = g_{11a} + g_{11b} \\
g_{12e} = g_{12a} + k_g g_{12b} \\
g_{21e} = g_{21a} + g_{21b} \\
g_{22e} = g_{22a} + k_g g_{22b}
\]
The performance merits derived in Section (3.2) can now be applied directly to characterize the shunt-series feedback amplifier.

Shunt-series feedback generally entails the interconnection of an active structure, Network \( A \), with a passive unit, Network \( B \). In this case, \(|g_{21a}| >> |g_{21b}|\) and \(|g_{12a}| << |k_g g_{12b}|\). This is to say that the input-to-output, or forward, signal path is dominated by the gain afforded by the active structure, while the feedback subcircuit is designed to ensure that it dominates the output-to-input, or feedback signal flow path. From Section (3.2), a large loop gain delivers a resultant closed loop current gain, \( A_i \), of
\[
A_i = \frac{I_2}{I_s} \approx \frac{1}{g_{12e}} \approx \frac{1}{k_g g_{12b}}
\]
which is nominally independent of parametric vagaries inevitably encountered in active circuits. Moreover, large loop gain produces a driving point input admittance, \( Y_{in} \), of
\[
Y_{in} = -\frac{k_g g_{12b} g_{21a}}{g_{22a} + k_g g_{22b} + Z_l}
\]
and a driving point output impedance, \( Z_{out} \), given approximately by
\[
Z_{in} = -\frac{k_g g_{12b} g_{21a}}{g_{11a} + g_{11b} + Y_s}
\]
The negative algebraic signs appearing on the right hand sides of the preceding two expressions are not a concern in unconditionally stable shunt-series systems, which have \( k_g g_{12b} g_{21a} < 0 \) for at least low signal frequencies.

4.3. SHUNT-SHUNT FEEDBACK

In the shunt-shunt feedback architecture of Figure (42a), y-parameters comprise the most expeditious analytical vehicle. The structure at hand produces low input impedance and low output impedance, thereby rendering it suitable for transimpedance applications. Armed
with the experiences gleaned from the preceding two considered feedback architectures, it is easily demonstrated that the pertinent \( y \)-parameter equivalent circuit is the model in Figure (42b), where the effective \( y \)-parameters, \( y_{ij_e} \), are

\[
\begin{align*}
    y_{11e} &= y_{11a} + y_{11b} \\
    y_{12e} &= y_{12a} + y_{12b} \\
    y_{21e} &= y_{21a} + y_{21b} \\
    y_{22e} &= y_{22a} + y_{22b}
\end{align*}
\]  

(121)

If Network \( A \) is an active circuit and Network \( B \) is a passive structure, \( |y_{21a}| >> |y_{21b}| \) and \( |y_{12a}| << |y_{12b}| \) for reasons analogous to those proffered in conjunction with the shunt-series amplifier. Under these conditions and for large loop gain, the closed loop transimpedance can be shown to be given by

\[
Z_f = \frac{V_2}{I_s} \approx \frac{1}{y_{12e}} \approx \frac{1}{y_{12b}}.
\]  

(122)

Moreover, the driving point input and output admittances respectively become
\[ Y_{in} = -\frac{y_{12b}y_{21a}}{y_{22a} + y_{22b} + Y_l}, \quad (123) \]

and

\[ Y_{out} = -\frac{y_{12b}y_{21a}}{y_{11a} + y_{11b} + Y_s}. \quad (124) \]

4.4. SERIES-SERIES FEEDBACK

In the series-series feedback system of Figure (43a), Thévenin equivalent I/O port models, and thus z-parameter modeling is appropriate. The considered system at hand produces high input and output driving point closed loop impedances, whence the system functions as a transadmittance amplifier. As is the case with the series components of the series-shunt and shunt-series amplifiers, note that the input and output port currents of Network B are indicated as respectively proportional to the input and output port currents of the presumably active subcircuit, Network A. The applicable z-parameter equivalent circuit is provided in Figure (43b), where the effective z-parameters, \( z_{j\ell k} \), are

![Series-Series Feedback Interconnection Of Two Linear Two Port Networks](image)

Fig. (43). (a). Series-Series Feedback Interconnection Of Two Linear Two Port Networks. (b). The z-Parameter Equivalent Circuit Of The System In (a).
Assuming large loop gain, $|z_{21a}| >> |k_iz_{11b}|$, and $|z_{12a}| << |k_oz_{12b}|$, the closed loop transadmittance is

\[
Y_f = \frac{I_2}{V_s} = \frac{1}{z_{12e}} \approx \frac{1}{k_oz_{12b}},
\]

(126)

the closed loop input impedance is

\[
Z_{in} \approx -\frac{k_iz_{12b}z_{21a}}{z_{22a} + k_oz_{22b} + Z_l},
\]

(127)

and the closed loop output impedance is

\[
Z_{out} \approx -\frac{k_iz_{12b}z_{21a}}{z_{11a} + k_iz_{11b} + Z_s}.
\]

(128)

5.0. REFERENCES


