Overview Of Lecture

- **Biasing Requirement**
  - Active Regime For Nominal I/O Linearity
  - Predictable Quiescent Collector Current
    - Dependence Of Small Signal Parameters On Current
    - Thermal Sensitivity Issues
    - Sensitivity Problems Related To Current Gain Variations

- **Bipolar Biasing Architectures**
  - Passive Biasing Networks
    - World’s Worst Biasing Circuit
    - Current-Controlled Current Feedback
  - Active Biasing Networks
    - Diode Current Mirror
    - Diode-Resistor Current Mirror
    - $V_{be}$ Multiplier Biasing
    - N-Stage Current Mirror
    - Wilson Current Mirror

- **Supply-Independent Biasing**
  - Conventional Network
  - Bandgap Reference Cell
Biaseding Premise

- **Primary Purpose**
  - Achieve Nominal I/O Linearity For Signal Processing Purposes
  - Necessary Condition Is Forward Active Regime Biasing

- **Fundamental Biasing Requirement**
  - $V_{beQ} > V_{eon}$ & $V_{ceQ} \geq V_{beQ}$
    - Accurate And Predictable Collector Q-Point Current, $I_{cQ}$
    - Reasonably Accurate Collector-Emitter Q-Point Voltage, $V_{ceQ}$
      - Small Signal Parameters Are Very Sensitive To $I_{cQ}$
      - Small Signal Parameters Are Somewhat Sensitive To $V_{ceQ}$

- **Fundamental Biasing Issues**
  - “DC” Gain $h_{FE}$ Is Very Unpredictable
    - Shows Wide Variance For Given Transistor At Specified Q-Point
    - Somewhat Variant With Temperature
    - $I_{cQ}$ Must Not Be Rendered Directly Proportional To $h_{FE}$
  - Collector Current Displays Propensity For Increasing With Junction Operating Temperature, $T_j$
    - Renders All Small Signal Parameters Vulnerable
    - Compensate By Allowing For Decrease In $V_{beQ}$ Over Temperature
      - $\Delta V_{beQ} = -S_{be} \cdot \Delta T_j$
      - $S_{be}$ Of Order of 2 -To- 4 mV/°C
Pre-Design Comments And Guidelines

- **Device Matching**
  - On Chip Physical Matching Of Transistors Is Easy To Achieve
  - Electrical Matching
    - Requires Approximately the Same (Or Similar) Collector-Emitter Voltages
    - Requires Identical Current Densities
      \[ J_{ci} = J_{ck} \] (Collector Current Densities)
      \[ I_{ci}/A_{ei} = I_{ck}/A_{ek} \] (Collector Current In Terms Of Emitter Areas)
    - Gives Matched Quiescent Currents That Track Over Temperature
    - Facilitates Predictability Of Biasing Levels And Other Circuit Metrics
    - Forward Biasing For Linear Signal Processing Applications
    - Critical Devices Must Be Laid Out In Close Proximity To Help Ensure That Devices Experience Nominally The Same Temperatures

- **Basic Requirements For Quality Biasing Design**
  - The Foregoing Matching Stipulations
  - Resistors With Low Temperature Coefficients
  - Resistor Ratios With Very Low Temperature Coefficients
  - Power Supply Voltages That Are Nominally Invariant With Temperature
World’s Worst BJT Biasing Circuit

- **Circuit Diagram**
  - **High Level**
    - For Large $h_{FE}$, Q-Point Base Current, $I_{cQ}/h_{FE}$ Is Near Zero
    - Voltage $V_{beQ}$ Is Rendered Constant At $R_2 V_{cc}/(R_1 + R_2)$
    - Not Good For Temperature Sensitivity Mitigation
  - **Analysis**
    - $I_{cQ}$ Directly Proportional To $h_{FE}$
    - $V_{beQ}$ Temperature Sensitivity Amplified
    - Assumes $h_{FE}$, $V_{cc}$, & Resistors Are Temperature Invariant
Current-Controlled Voltage Feedback

- **Circuit Diagram**

- **High Level**
  - For Large $h_{FE}$, $V_{bx}$ constant, given by divider off of $V_{cc}$
  - If $I_{cQ}$ increases, voltage $V_{re}$ across $R_{ee}$ increases
  - Result is decrease in $V_{beQ}$, which compensates for original increase in $I_{cQ}$
  - Works just as well when change in $I_{cQ}$ is a decrease for any reason

- **Analysis**
  - Via KVL
  - Result can be straightforwardly solved for the quiescent collector current, $I_{cQ}$

$$\left(\frac{R_2}{R_1 + R_2}\right)V_{cc} = \left(R_{I||R_2}\right)\left(\frac{I_{cQ}}{h_{FE}}\right) + V_{beQ} + \left(\frac{h_{FE} + 1}{h_{FE}}\right)R_{ee}I_{cQ}$$
Current-Controlled Feedback . . . Cont’d

- **Quiescent Collector Current**

\[
I_{cQ} = h_{FE} \left( \frac{R_2}{R_1 + R_2} \right) \left[ V_{cc} - \left( 1 + \frac{R_1}{R_2} \right)V_{beQ} \right] \frac{1}{(R_1 || R_2) + (h_{FE} + 1)R_{ee}}
\]

- **Design Considerations**
  - Reduce Current Dependence On \( h_{FE} \)
    \[
    (R_1 || R_2) << (h_{FE} + 1)R_{ee}
    \]
    \[
    I_{cQ} \approx \left( \frac{\alpha_{FE}}{R_{ee}} \right) \left( \frac{R_2}{R_1 + R_2} \right) \left[ V_{cc} - \left( 1 + \frac{R_1}{R_2} \right)V_{beQ} \right]
    \]
  - Temperature Sensitivity Of Collector Current
    \[
    \sigma_i \triangleq \frac{\Delta I_{cQ}}{\Delta T_j} \approx -\left( \frac{\alpha_{FE}}{R_{ee}} \right) \left( \frac{R_2}{R_1 + R_2} \right) \left( 1 + \frac{R_1}{R_2} \right) \frac{\Delta V_{beQ}}{\Delta T_j} = \frac{\alpha_{FE} S_{be}}{R_{ee}}
    \]
  - Temperature Sensitivity Assumes Resistors, Power Supply, And \( h_{FE} \) Are Temperature Invariant
Comments On Current-Controlled Biasing

- **Mitigation Of $h_{FE}$ Uncertainties**
  - Inequality Renders $I_{cQ}$ Dependent On $\alpha_{FE}$, Not $h_{FE}$
  - Desired Biasing Accuracy Determines Nature Of Inequality
    - 10% Biasing Error Requires $R_1 || R_2 \leq (h_{FE} + 1)R_{ee}/10$
    - 1% Biasing Error Requires $R_1 || R_2 \leq (h_{FE} + 1)R_{ee}/100 - - -$ etc.

- **Mitigation Of Temperature Sensitivity**
  - Resistance $R_{ee}$ Is Pivotal
  - Larger $R_{ee}$ Results In Decreased Temperature Sensitivity, $\sigma_i$
    - Reasonable In That $R_{ee}$ Produces Corrective Voltage $V_{re}$ In Response To Perturbation In $I_{cQ}$
    - Too Large Of An $R_{ee}$ Value Is Undesirable
      - Requires Large Biasing Supply, $V_{cc}$ To Ensure Forward Active Biasing
      - Diminishes Forward Voltage/Power Gain Of Amplifier
      - Increases Power Dissipation

- **Another Measure Of Biasing Quality**
  - Current $I_{cQ}$ Should Ideally Be Invariant With Changes In $V_{ceQ}$
  - Measure Of This Quality Is Small Signal Impedance, $Z_x$
    - Very Large $Z_x$ Implies Approximate Ideal Current Source Output Port
    - Ideal Current Source Is Independent Of Its Port Voltage
Current-Controlled Output Impedance

- Low Frequency Small Signal Model
- Circuit Analysis
  - Equilibrium Equations
    \[ 0 = \left( R_1 \parallel R_2 + r_{bb} + r_\pi + R_{ee} \right) I + R_{ee} I_x \]
    \[ V_x = \left( r_o + R_{ee} \right) I_x - \left( \beta_{ac} r_o - R_{ee} \right) I \]
  - Analytical Results
    \[ R_X = \frac{V_x}{I_x} = R_{ee} \left( R_1 \parallel R_2 + r_{bb} + r_\pi \right) + \left( 1 + \frac{\beta_{ac} R_{ee}}{R_{ee} + R_1 \parallel R_2 + r_{bb} + r_\pi} \right) r_o \]
    \[ \approx \left( 1 + \frac{\beta_{ac} R_{ee}}{R_{ee} + R_1 \parallel R_2 + r_{bb} + r_\pi} \right) r_o \]
    At Low Signal Frequencies, Impedance \( Z_x \) Reduces To A Simple Resistance, \( R_x \)
  - Discussion
    - Large \( R_{ee} \) Potentially Forges \( R_x \) Considerably Larger Than Early Resistance \( r_o \)
    - \( R_{ee} = 0 \) Delivers \( R_x = r_o \)
      - As Expected
      - Reasonably Large But Not Nearly As Large As \( R_x \) When \( R_{ee} > 0 \)
Diode-Resistor Current Mirror

- **Circuit Diagram**
  - Q1 and Q2 must be matched transistors, save possibly for differences in emitter-base junction areas.
  - Equality between the two base-emitter voltages, \( V_{beQ} \), requires equal current densities in Q1 and Q2.

- **Circuit Analysis And Results**
  - Emitter current of Q1 mirrors Q2 emitter current by factor of \( R_2/R_{ee} \).
  - Stabilization of \( I_{cQ} \) reduces to problem of stabilizing \( I_{dQ} \).

Mathematical expressions:

\[
\frac{I_{dQ}}{A_{e2}} = \left( \frac{h_{FE} + 1}{h_{FE}} \right) \frac{I_{cQ}}{A_{e1}}
\]

\[
V_{beQ} + R_2 I_{dQ} = V_{beQ} + \left( \frac{h_{FE} + 1}{h_{FE}} \right) R_{ee} I_{cQ}
\]

\[
I_{cQ} = \left( \frac{h_{FE}}{h_{FE} + 1} \right) \left( \frac{R_2}{R_{ee}} \right) I_{dQ} \approx \left( \frac{R_2}{R_{ee}} \right) I_{dQ}
\]

\[
V_{beQ} + \left( \frac{h_{FE} + 1}{h_{FE}} \right) I_{cQ} = V_{beQ} + I_{cQ}/h_{FE}
\]
Diode-Resistor . . . Cont’d

- **Circuit Analysis And Results, Cont’d**
  - Current Mirror Relationship
    
    \[
    I_{cQ} = \left( \frac{h_{FE}}{h_{FE} + 1} \right) \left( \frac{R_2}{R_{ee}} \right) I_{dQ} \approx \left( \frac{R_2}{R_{ee}} \right) I_{dQ}
    \]
  - Quiescent Collector Current
    
    \[
    I_{cQ} = h_{FE} \left( \frac{R_2}{R_1 + R_2} \right) \left[ \frac{V_{cc} - V_{beQ}}{(R_1 || R_2) + (h_{FE} + 1)R_{ee}} \right]
    \]
  - Design Considerations
    - Resultant Current
      \[
      I_{cQ} \approx \alpha_{FE} \left( \frac{R_2}{R_1 + R_2} \right) \left( \frac{V_{cc} - V_{beQ}}{R_{ee}} \right)
      \]
    - Thermal Sensitivity
      \[
      \sigma_i \triangleq \frac{\Delta I_{cQ}}{\Delta T_j} \approx \frac{\alpha_{FE}S_{be}}{R_{ee}} \left( \frac{R_2}{R_1 + R_2} \right) = \frac{I_{cQ}S_{be}}{V_{cc} - V_{beQ}}
      \]

  - Smaller Than Thermal Sensitivity Of Current Feedback Network
  - Low Sensitivity Determined Largely By Power Supply Voltage, \( V_{cc} \)
    - Resistance \( R_{ee} \) Is Non-Critical For Sensitivity Purposes
    - Larger Voltages (Larger Power Dissipation) Imply Enhanced Performance
Diode-Resistor Output Resistance

- **Output Resistance Computation**
  - Can Rely On Current Feedback Results
    - Replace $R_2$ Therein By $(R_2 + R_d)$
    - $R_d$ Is Resistance Of Diode-Connected Q2
  - Basic Result
    \[
    R_x = R_{ee} \left[ \frac{R_1}{R_2 + R_d + r_{bb} + r_\pi} \right] + \left( 1 + \frac{\beta_{ac} R_{ee}}{R_{ee} + R_1 \left( R_2 + R_d + r_{bb} + r_\pi \right)} \right) r_o \\
    \approx \left( 1 + \frac{\beta_{ac} R_{ee}}{R_{ee} + R_1 \left( R_2 + R_d + r_{bb} + r_\pi \right)} \right) r_o
    \]

- **Diode $R_d$**
  \[
  R_d = \frac{V_x}{I_x} = r_o \left( \frac{r_{bb} + r_{\pi}}{\beta_{ac} + 1} \right) \approx r_{bb} + r_{\pi} \]

Output Resistance Is Essentially The Same As That For Current Feedback Architecture
Diode Current Mirror

- Circuit Diagram
  - Same As Previous Circuit But Without Resistances In Emitters Of Transistors
  - Transistors Are Matched
    - Area Of Q1 Is \( k \)-Times That Of Q2
    - Resultant Current Relationship
  - Approximation Requires \( (h_{FE} + 1) >> k \), Which Is Assured
  - Comparison To Diode Resistor Architecture
    - Temperature Sensitivity Is Identical To Diode-Resistor Circuit
    - Smaller Surface Area Because Of Absence Of Series Resistances
    - Lower Power Dissipation Because Of No Series Resistances

\[
k I_{dQ} = \left(\frac{h_{FE} + 1}{h_{FE}}\right) I_{cQ}
\]

\[
I_{cQ} = \frac{h_{FE} (V_{cc} - V_{beQ})}{R \left(1 + \frac{h_{FE} + 1}{k}\right)} \approx \frac{\alpha_{FE} k (V_{cc} - V_{beQ})}{R}
\]
**V_{be}**-Multiplier Circuit Cell

- **Circuit Cell Diagram**
  - Applications
    - Static (“DC”) Level Shifting
    - Thermally Compensated BJT Biasing
  - Applied Current $I_m$ Must Place Transistor Q2 In Its Forward Active Domain

- **Circuit Analysis**
  - Equilibrium Equations
  - Eliminate Current $I_{c2}$
    \[ V_m = k_m V_{be2} + R_m I_m \]
  - Circuit Interpretation
    - Open Circuit Terminal Voltage Is Multiplied (By Factor Of $k_m$) Version Of $V_{be}$
      - Multiplication Factor ($k_m$) Is Roughly ($1 + R_y/R_x$)
      - $\alpha_{FE2}$ Is Almost One Because Of Large $h_{FE2}$
    - Resistance $R_m$ Is Small
      - Large $h_{FE2}$
      - Circuit Behaves Resultantly As Approximation Of Voltage Source
Small Signal $V_{be}$-Multiplier Resistance

### Circuit And Model
- Transistor Is Biased In Forward Active Mode
- Network Acts As A Linear Two-Terminal Structure
- At Low Frequencies Network Is Necessarily A Linear Resistance, $R_y$

### Circuit Analysis And Results
- $R_y = 0 \& R_x = \infty$ Reduces $R_v$ To $R_d$ (Bipolar Diode Resistance)
- $R_y = 0$ Reduces $R_v$ To Shunt Combination Of $R_d$ And $R_x$, As Expected
- In General, $R_v$ Is Slightly Larger Than $R_d$

\[
V_x = R_y \left( I_x - \beta_{ac2} I \right) + (r_{bb2} + r_{\pi2}) I
\]

\[
R_v = \frac{V_x}{I_x} = \left( 1 - \frac{\alpha_{ac2} R_x}{R_x + R_d} \right) R_y + R_x \parallel R_d
\]

\[
R_d = \frac{V_x}{I_x} = r_{o2} \left( \frac{r_{bb2} + r_{\pi2}}{\beta_{ac2} + 1} \right) \approx \frac{r_{bb2} + r_{\pi2}}{\beta_{ac2} + 1}
\]

\[
a_{ac2} = \frac{\beta_{ac2}}{\beta_{ac2} + 1}
\]
V_{be} - Multiplier Mirror Biasing

- Circuit And Alternative Form For Static Analysis
- Design Requirement
  - Matched Transistors
  - Matched Transistor Current Densities
    - \( I_{cQ}/A_{e1} = I_{c}/A_{e2} \)
    - Then \( V_{be2} = V_{beQ} \)
    - Differing Currents Mandate Appropriately Scaled Emitter-Base Junction Areas
  - Matching Devices And Densities Imply \( h_{FE1} = h_{FE2} \triangleq h_{FE} \)
**V_{be}-Multiplier Mirror Results**

- **Equilibrium Equations**
  \[
  V_{cc} = R_1 \left( I_m + \frac{I_{cQ}}{h_{FE}} \right) + (R_2 + R_m) I_m + k_m V_{beQ}
  \]

- **Resultant Quiescent Collector Current**
  \[
  (R_2 + R_m) I_m + k_m V_{beQ} = R_{ee} \left( \frac{h_{FE} + 1}{h_{FE}} \right) I_{cQ} + V_{beQ}
  \]

- **Design Requirements**
  - Desensitize w/r To $h_{FE}$
  - Desensitize w/r To $V_{beQ}$ (Temperature)

- **Design Result**
  \[
  I_{cQ} = h_{FE} \left( \frac{R_2 + R_m}{R_1 + R_2 + R_m} \right) \left\{ \frac{V_{cc} - \left[ 1 - \frac{(k_m - 1) R_1}{R_2 + R_m} \right] V_{beQ}}{R_1 \left[ (R_2 + R_m) + (h_{FE} + 1) R_{ee} \right]} \right\}
  \]

\[
R_1 \left( R_2 + R_m \right) << \left( h_{FE} + 1 \right) R_{ee}
\]

\[
k_m - 1 = \frac{\alpha_{FE2} R_y}{R_x} = \frac{R_2 + R_m}{R_1} \Rightarrow \frac{R_y}{R_x} \approx \frac{R_2}{R_1}
\]

\[
I_{cQ} \approx \left( \frac{R_2 + R_m}{R_1 + R_2 + R_m} \right) \left( \frac{\alpha_{FE} V_{cc}}{R_{ee}} \right) \approx \left( \frac{R_2}{R_1 + R_2} \right) \left( \frac{V_{cc}}{R_{ee}} \right)
\]
Comments On $V_{be}$-Multiplier Mirror

- **Quiescent Collector Current**
  - Nominally Independent Of Transistor Parameters And Metrics
  - Accordingly, Nominally Insensitive To:
    - Device Operating Temperature
    - Device Processing Uncertainties
    - Assumes
      - Assume Power Supply $V_{cc}$ Is Stable As Well As Resistance $R_{ee}$
      - Assumes Resistance Ratios $R_x/R_y$ And $R_1/R_2$ Are Stable
  
- **Small Signal Out Resistance, $R_x$**
  - Nominally The Same As For Current Feedback Architecture
  - Need Only Replace $R_2$ In Current feedback By $(R_2 + R_v)$
  - Result (Relatively Large Output Port Resistance)

$$
R_x = R_{ee} \left[ R_1 \left( R_2 + R_v \right) + r_{bb} + r_\pi \right] + \left( 1 + \frac{\beta_{ac} R_{ee}}{R_{ee} + R_1 \left( R_2 + R_v \right) + r_{bb} + r_\pi} \right) r_o
$$

$$
\approx \left( 1 + \frac{\beta_{ac} R_{ee}}{R_{ee} + R_1 \left( R_2 + R_v \right) + r_{bb} + r_\pi} \right) r_o
$$
N-Stage Current Mirror

- **Common Embodiment**
  - Uses One Diode Reference (Q0) For Several Current Sinks (Or Sources)
  - Application
    - Biasing Of Several Subcircuits
    - Multiple Active Loads
  - Transistors
    - All Transistors Matched
    - $k_i$ Represents Ratio Of Emitter-Base Junction Area Of Qk To Area Of Q0

- **Analysis**
  - Reference Current
    $$I_r = I_o + \sum_{i=1}^{N} (1 - a_{FE}) I_o \cdot k_i$$
  - Collector Current In $k^{th}$ Transistor
    $$I_{ck} = \frac{a_{FE} k_k I_r}{1 + (1 - a_{FE}) \sum_{i=1}^{N} k_i} = \frac{a_{FE} k_k (V_{cc} - V_{be})}{R}$$
N-Stage Current Mirror Design

- **Static Current Responses**

- **Design Metrics**
  - Reduction Of Gain Sensitivity
    - High $h_{FE}$ Is A Necessity
    - Restriction Imposed On Number Of Current Stages
  - Temperature Sensitivity Is Identical To Diode Mirror Biasing

- **Output Resistance**
  - $R_{xk}$ Is Obviously $r_{ok}$, The Early Resistance Of $k^{th}$ Transistor
  - Generalized Expression

\[
I_{ck} = \frac{\alpha_{FE} k_i I_r}{1 + (1 - \alpha_{FE}) \sum_{i=1}^{N} k_i} = \frac{\alpha_{FE} k_i (V_{cc} - V_{be})}{1 + (1 - \alpha_{FE}) \sum_{i=1}^{N} k_i} R
\]

\[
\sum_{i=1}^{N} k_i << \frac{1}{1 - \alpha_{FE}} = (h_{FE} + 1)
\]

\[
R_{xk} = r_{ok} \approx \frac{V_{kQ} + V_{af}}{I_{ck}} \approx \left[ \frac{V_{kQ} + V_{af}}{\alpha_{FE} k_i (V_{cc} - V_{be})} \right] R
\]

- Gain Sensitivity Constraint Is Presumed Satisfied
- Too High A Reference Current (Small $R$) Compromises Current Stage Output Port Resistance
Compensated N-Stage Current Mirror

- **Circuit Diagram**
  - Compensation Entails Introduction Of Transistor $Q_P$
  - Transistor $Q_P$ Isolates Reference Current $I_r$ From Collector Current Sinking Currents
  - Generally, Resistance $R_p$ Is Adjustable
    - Goal Is $I_p \approx I_o$
    - Goal Is Identical Current Densities Throughout So That All $V_{be}$’s Are Nominally The Same

- **Circuit Results For $I_p = I_o$**
  - Temperature Stability Somewhat Compromised Because Of Dependence On $2V_{be}$
  - Note $I_r \approx I_o$ Since $(1-\alpha_{FE})^2 \approx 1$

\[
I_r = I_o \left[ 1 + (1-\alpha_{FE})^2 \left( 1 + \sum_{i=1}^{N} k_i \right) \right] \approx I_o
\]

\[
I_{ck} \approx \alpha_{FE} k_k I_o \approx \frac{\alpha_{FE} k_k (V_{cc} - 2V_{be})}{R}
\]
Wilson Current Mirror

- **Circuit Diagram**
  - Q2-Q3 Serves As Convention Diode Mirror
  - Q2-Q1 Is Analogous To The N-Stage Enhancement Discussed In Preceding Slide

- **Simplified Analysis**
  - Very Large $h_{FE}$ (Ignore Base Currents)
  - Reference Current Is $I_r$
    \[
    I_r = \frac{V_{cc} - V_{be1} - V_{be2}}{R} = \frac{V_{cc} - 2V_{be}}{R}
    \]
    - Approximation Entails Identical Devices Conducting Identical Current Densities
    - Typical Tactic In Bipolar Integrated Circuit Biasing Design
  - $I_r = I_2$ (Ignoring Base Current) $\rightarrow I_{e3} = kI_2 = kI_r$ (Given Area Factor)
  - $I_1 = I_{e1} = kI_2 = kI_r$
  - Note Then That $I_1/I_r = k$ (Current Gain Controlled Geometrically)
  - Thermal Sensitivity Entails $2V_{be}$ Dependence (Similar To Compensated N-Stage Current Mirror)
    \[
    I_r \approx k \left( \frac{V_{cc} - 2V_{be}}{R} \right)
    \]
Wilson Mirror Static Analysis

- **Circuit Diagram**

- **Equilibrium Equations**

  \[ I_{e1} = kI_2 + \left(1 - \alpha_{FE}\right)I_2 \]

  \[ I_1 = \alpha_{FE}kI_2 \left(1 + \frac{1 - \alpha_{FE}}{k}\right) \]

  \[ I_{b1} = \frac{I_1}{h_{FE}} = \left(1 - \alpha_{FE}\right)kI_2 \left(1 + \frac{1 - \alpha_{FE}}{k}\right) \]

  \[ I_r = I_{b1} + \alpha_{FE}I_2 = \alpha_{FE}I_2 \left[1 + \left(\frac{k}{h_{FE}}\right)\left(1 + \frac{1 - \alpha_{FE}}{k}\right)\right] \]

- **Static Collector Current Response (Identical Devices With Identical Current Densities)**

  \[ I_1 = \frac{kI_r \left(1 + \frac{1 - \alpha_{FE}}{k}\right)}{1 + \frac{k}{h_{FE}} + \frac{1}{h_{FE} \left(h_{FE} + 1\right)}} \approx kI_r \]

  \[ I_1 = \frac{kI_r \left(1 + \frac{1}{h_{FE} + 1}\right)}{1 + \frac{k}{h_{FE}} + \frac{1}{h_{FE} \left(h_{FE} + 1\right)}} = \frac{kI_r}{1 + \frac{k}{h_{FE}} + \frac{1}{h_{FE} \left(h_{FE} + 1\right)}} \approx kI_r \]
Wilson Mirror Small Signal Analysis

- **Preliminaries**
  - Q1 & Q3 Conduct Virtually Identical Currents
  - Short Circuit Gains Are Virtually Current Invariant
  \[ \beta_{ac1} \approx \beta_{ac2} \approx \beta_{ac3} \triangleq \beta_{ac} \]
  - Diode-Connected Transistor Q2

- **Diode Q2**
  - Two Terminal Element Behaving As A Resistance At Low Signal Frequencies
  - Resistance Has Been Previously Evaluated
  \[ R_{d3} = r_{o3} \left( \frac{n_{bb3} + r_{\pi3}}{\beta_{ac3} + 1} \right) \approx r_{o} \left( \frac{n_{bb} + r_{\pi}}{\beta_{ac} + 1} \right) \approx \frac{n_{bb} + r_{\pi}}{\beta_{ac} + 1} \]

- **The Foregoing Disclosures Can Be Exploited To Forge A Meaningful Equivalent Circuit From Which The Output Port Resistance, \( R_x \) Can Be Determined Via The **Mathematical Ohmmeter Method**

\[ n_{bb1} \approx n_{bb3} \triangleq n_{bb} \]
\[ r_{\pi1} \approx r_{\pi3} \triangleq r_{\pi} \]
\[ r_{o1} \approx r_{o3} \triangleq r_{o} \]
\[ n_{bb2} \approx kr_{bb3} = kr_{bb} \]
\[ r_{\pi2} \approx kr_{\pi3} = kr_{\pi} \]
\[ r_{o2} \approx kr_{o3} = kr_{o} \]

\[ R_{ss} \triangleq (r_{o2}) \left\| R = (kr_{o}) \right\| R \approx R \]
Wilson Mirror Output Resistance

- Low Frequency Small Signal Model
- Analytical Expression

\[ R_x = R_{ss} + \frac{\alpha_{ac} \beta_{ac} R_{ss} + k \left( \frac{r_{bb} + r_{\pi}}{\beta_{ac} + 1} \right)}{(k + 1) R_{ss} + \left[ 1 + k (\beta_{ac} + 2) \right] \left( \frac{r_{bb} + r_{\pi}}{\beta_{ac} + 1} \right)} r_o \]

- Approximate Result (Relies On Large \( \beta_{ac} \))

\[ R_x \approx \left[ 1 + \frac{\beta_{ac} R_{ss}}{(k + 1) R_{ss} + k \left( r_{bb} + r_{\pi} \right)} \right] r_o \]
Supply-Independent Biasing

**Premise**
- Conventional Biasing Discussed Thus Far Relies On Accurately Predictable, Stable, And Thermally Insensitive Supply Voltage
- Presumptions Are Not Realistic, Particularly For Portable Electronics
- Solution Is Biasing Rendered Independent Of Power Supply Voltage Over Suitable Range Of Operation

**Schematic Depiction**
- PNP Devices Must Be Matched, Save For Area Ratio, $k_p$, Of Q5
- NPN Devices Must Be Matched, Save For Area Ratio, $k_n$, Of Q2
- All Transistors Must Operate In Their Forward Active Regimes, Regardless Of $V_{cc}$ Fluctuation
  - Sets Dynamic Range Of Network
  - Output Resistance $R_x$ Presumes Forward Active Operation Of All Transistors
Supply-Independent Analysis

**Observation**

\[ IQ = I_s \left[ e^{V_{be1}/n_fV_T} - 1 \right] = k_n I_s \left[ e^{V_{be2}/n_fV_T} - 1 \right] \]

\[ IQ \approx I_s e^{V_{be1}/n_fV_T} \approx k_n I_s e^{V_{be2}/n_fV_T} \]

\[ V_{be1} - V_{be2} \approx n_fV_T \ln(k_n) \]

**Results**

- Assumes Large \( h_{FE} \)
- Base Currents Are Effectively Ignored
- Currents \( I_Q \) And \( I_o \) Are Independent Of \( V_{cc} \)
  - Assumes All Transistors Operate In Forward Active Regime
  - Requirements
    - Minimum Value Of \( V_{cc} \) Must Be Sufficiently Large
    - Resistances \( R_{ee}, R, \) and \( R_l \) Cannot Be Excessively Large
Supply-Independent Design

- **Forward Active Regime Biasing**
  - Transistors Q1 and Q3 Automatically In Forward Active Domain
  - Transistor Q4
    \[ V_{ee4} \geq V_{eb4} \Rightarrow V_{cc} \geq R_{ee} I_Q + V_{be1} + V_{eb4} \]
  - Transistor Q2
    \[ V_{ce2} = V_{cc} - V_{eb3} - (R_{ee} + R) I_Q \geq V_{be2} \Rightarrow V_{cc} \geq R_{ee} I_Q + V_{be2} + V_{eb3} + n_f V_T \ln(k_n) \]
  - Satisfaction of first inequality basically requires \( V_{cc} \geq 1.5 \) Volts
  - Satisfaction of second inequality automatically satisfies first inequality

- **Constant Transconductance \((g_m)\) Cells**
  - Devices Q1, Q2, Q3, Q4
    - Implies plausibility of temperature-invariant gain in these cells
    - **Constant \(g_m\)** is achieved because circuits display collector currents that are **PTAT** (proportional to absolute temperature)
  - **PTAT** attribute extends to Q5

\[
\begin{align*}
g_{m1} &= g_{m2} = g_{m3} = g_{m4} \approx \frac{I_Q}{n_f V_T} \approx \frac{\ln(k_n)}{R} \\
I_Q &\approx \frac{n_f V_T \ln(k_n)}{R} = \frac{n_f k T J \ln(k_n)}{qR} \\
g_{m5} &\approx \frac{I_o}{n_f V_T} \approx \frac{k_p I_Q}{n_f V_T} \approx \frac{k_p \ln(k_n)}{R}
\end{align*}
\]
Supply-Independent Startup

- Problem
  - Mathematically Viable Circuit Solution Is $I_Q = I_o = 0$
  - Circuit Fundamentally Latches Into Null Startup State
    - Common Problem In Almost All Supply-Independent Bias Schemes
    - Problem Mitigation
      - Passive Compensation Entails Introduction Of Large Resistance Between Ground And Collector Of Either $Q_1$ Or $Q_2$ To Foster Inherent Circuit Imbalance
        - Problem Is That Compensation Remains Forever Conductive
        - Low Steady State Power Requires Large Compensation Resistance
        - Large Resistances Are Inherently Inaccurate, But Accurate Resistance Value Is Not Required
      - Inherently Imperfect Device Matching May Be Sufficient Imbalance To Obviate Startup Shortfalls
      - Active Compensation Preferred
        - Sufficient Imbalance Is Assured
        - Does Not Conduct In Steady State
        - Does Require Two Additional Transistors
        - Does Require Reasonable Large On-Chip Capacitance

- Circuit Diagram And Engineering Analysis On Following Slides
Supply-Independent Startup Cell

- Circuit Diagram
- Operation
  - At Time $t = 0$, Voltage $V_p(t)$ Approximates An Ideal Voltage Step
  - Assuming Capacitance $C$ Is Initially Uncharged, $V_{cc}$ Appears At Q7 Base
  - Large Collector Current Flows Through Q7
  - Q7 Current Must Derive From Q3
  - Q3 Current Is Mirrored To Transistor Q4
  - Q4 Current Flows Through Q1 And Increases Voltage $V_{be1}$
  - Operational Description Continues On Next Slide
Startup Cell . . . Cont’d

- **Operation, Cont’d**
  - Voltage $V_{be2}$ Remains Low Because Q7 Sucks Current From Q3 And Starves Collector Of Q2
  - Transistor Q6 Commences Conduction
    - Q6 Collector Current Supplied By Capacitive Branch
    - Capacitor Current Continues To Flow Until C Charges To $V_c = V_{cc}$
  - Transistor Q7 Drops Below Threshold Requirement
    - Q7 And Q6 Are Starved Of Current
    - Q3 Current Must Now Flow Through Q2
    - Steady State Achieved Without Current In Startup Cell

- **Temporarily Achieves Imbalance Between Q3 And Q4 Circuit Legs**
Supply-Independent Sample Design

- Circuit Diagram
- Design Noted
  - Resistances Are In Units Of Ohms
  - Capacitance Is In Units Of Picofarads
  - Numbers In Yellow Boxes Are Steady State Nodal Voltages w/r To Ground
    - Simulated Values Are Delineated
    - Spice Parameters On Following Slides
## PNP Transistor SPICE Model Parameters

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<tr>
<th>SYMBOL</th>
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<th>DESCRIPTION OF PARAMETER</th>
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### NPN Transistor SPICE Model Parameters

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Output Currents -VS- Supply Voltages

Currents Are Nominally Constant For $V_{cc} \geq 1.2$ Volts. Design Results Are Imperfect Because Of Finite Early Resistances In Transistors.
Thermal Sensitivity Of Currents

Current Sensitivity Is About $6.79 \mu A/\degree C$
Transient Current Responses

![Graph showing transient current responses with labels Io, Iq, Ic7, and Ic6.](image)
Bandgap Reference Circuit Concept

- **System Level Concept**
- **Operational Description**
  - Constant Current Source, $I_c$, Produces Base-Emitter Junction Voltage, $V_{be}$
  - Voltage $V_{be}$ Has Negative Temperature Coefficient; Decreases With Temperature Almost Linearly
  - **PTAT** Generator Delivers Output Voltage, $-KV_T = -K(kT_j/q)$, Which Is Proportional To Absolute Temperature
  - Reference Output Voltage $V_{ref} = A_v(V_{be} + KV_T)$
- **Design Requirement**
  - Assume Voltage Gain $A_v$ and Constant $K$ Are Temperature Invariant
  - Design So That Output Voltage $V_{ref}$ Displays Zero Temperature Coefficient ($TC = dV_{ref}/dT$) At Reference Temperature Of $T_o$

$$K = -\left( \frac{T_o}{V_{To}} \frac{dV_{be}}{dT} \right)_{T=T_o}$$
### Ebers-Moll Model Of Bipolar Transistor

- \( I_s \rightarrow \) Saturation Current Of Transistor
- \( A_j \rightarrow \) Base-Emitter Junction Area
- \( J_s \rightarrow \) Saturation Current Density \((I_s/A_j)\) Of Transistor
- \( \eta \rightarrow \) Junction Injection Coefficient
- \( V_T \rightarrow \) Boltzmann Voltage \((kT/q)\)

### Base-Emitter Junction Thermal Characteristics

\[
V_{be}(T) = V_{go} \left( 1 - \frac{T}{T_o} \right) + V_{beo} \left( \frac{T}{T_o} \right) + \eta V_T \ln \left( \frac{J_c}{J_{co}} \right) + m \ln \left( \frac{T_o}{T} \right)
\]

- \( V_{go} \rightarrow \) Silicon Bandgap Potential At Reference Temperature \( T_o \)
- \( V_{beo} \rightarrow \) Base-Emitter Voltage At Reference Temperature \( T_o \)
- \( J_c \rightarrow \) Collector Current Density \((I_c/A_j)\) At Operating Temperature \( T \)
- \( J_{co} \rightarrow \) Collector Current Density At Reference Temperature \( T_o \)
- \( m \rightarrow \) Empirical Constant \((\approx 2.30 \text{ For Silicon Technology})\)
PN Junction Thermal Properties

- **Base-Emitter Voltage**
  \[
  V_{be}(T) = V_{go} \left( 1 - \frac{T}{T_o} \right) + V_{beo} \left( \frac{T}{T_o} \right) + \eta V_T \left[ \ln \left( \frac{J_c}{J_{co}} \right) + m \ln \left( \frac{T_o}{T} \right) \right]
  \]

- **Design Goal**
  - Design Target Is To Implement \( J_c/J_{co} = T/T_o \)
  - Result Is Almost Linear Decrease Of \( V_{be} \) With Temperature
  - Temperature Coefficient Of \( V_{be} \) Is Almost Constant

  \[
  V_{be}(T) = V_{go} \left( 1 - \frac{T}{T_o} \right) + V_{beo} \left( \frac{T}{T_o} \right) - \eta(m - 1)V_T \ln \left( \frac{T}{T_o} \right)
  \]

  \[
  M_{be}(T) \triangleq \frac{dV_{be}(T)}{dT} = -\frac{V_{go} - V_{beo}}{T_o} - \frac{\eta k(m - 1)}{q} \left[ 1 + \ln \left( \frac{T}{T_o} \right) \right]
  \]

  - See Plot, Next Page (Assume \( m = 2.30, V_{beo} = 700 \text{ mV And } \eta = 1.0 \))
  - Numerical Examples
    - \( M_{be}(0 \text{ °C}) = -1.787 \text{ mV/°C} \)
    - \( M_{be}(100 \text{ °C}) = -1.822 \text{ mV/°C} \)
$V_{be}$ Temperature Coefficient

![Diagram showing the temperature coefficient of $V_{be}$]

$M_{be}(T) (mV/\text{degree C})$

Junction Temperature (degree C)

- Temperature Coefficient:
  - $-1.85$
  - $-1.83$
  - $-1.81$
  - $-1.79$
  - $-1.77$
  - $-1.75$

- Temperature Range:
  - 0 to 100 degrees C
PTAT Concept

### Basic Circuit
- Two Identical Bipolar Junction Transistors
- Biased At Different Currents Or At Different Collector Current Densities

### Base-Emitter Voltage Difference

- Constant Ratio Of Current Densities Conducted By Two Identical Bipolar Junction Transistors (BJTs)
- Difference In Resultant Base-Emitter Voltages Is Directly Proportional To Absolute Operating Temperature Of Junctions
- Presumes No Significant Thermal Gradient Between BJTs

\[
I_{c1} = \frac{A_j J_{c1}}{J_s} = A_j J_s e^{V_{be1}(T)/\eta V_T} \\
I_{c2} = \frac{A_j J_{c2}}{J_s} = A_j J_s e^{V_{be2}(T)/\eta V_T} \\
V_{be2}(T) - V_{be1}(T) = \eta V_T, \ln \left( \frac{J_{c2}}{J_{c1}} \right) = \left( \frac{\eta k}{q} \right) T \ln \left( \frac{J_{c2}}{J_{c1}} \right) = \eta V_{To} \left( \frac{T}{T_o} \right) \ln \left( \frac{J_{c2}}{J_{c1}} \right)
\]
Bandgap Reference Realization

- **Circuit Schematic Diagram**
  - **Description**
    - Q1-Q2 Are Identical, Save For Different Emitter-Base Junction Injection Areas
    - Negative Feedback Applied To Amplifier Via Q1-R1-R2
  - **Design Requirements**
    - Transistors Must Have Sufficiently Large “DC” Beta, $h_{FE}$, To Justify Tacit Neglect Of Static Base Currents
    - Amplifier Must Have Sufficiently Large Open Loop Gain To Forge $V_i \approx 0$
    - $V_i = 0 \Rightarrow I_1 = I_2$ (Identical Collector Currents)

- **Basic Analysis**
  - $I_1 = I_2 = \frac{V_{be2} - V_{be1}}{R_2}$
  - $V_{be2} - V_{be1} = \eta V_T \ln \left(\frac{I_2/A_{j2}}{I_1/A_{j1}}\right) = \eta V_T \ln \left(\frac{A_{j1}}{A_{j2}}\right) = PTAT$
**Bandgap Reference Output**

- **Reference Voltage**
  
  \[ V_{\text{ref}} = V_{\text{be2}} + 2I_1 R_1 = V_{\text{be2}} + \left( \frac{2R_1}{R_2} \right) \eta V_T \ln \left( \frac{A_{j1}}{A_{j2}} \right) \]

- **Recall TC Of Base-Emitter Voltage**
  
  \[ M_{\text{be}}(T) \triangleq \frac{dV_{\text{be}}(T)}{dT} = \frac{V_{\text{go}} - V_{\text{beo}}}{T_o} - \frac{\eta k (m-1)}{q} \left[ 1 + \ln\left( \frac{T}{T_o} \right) \right] \]

- **TC Of Reference Output Voltage**
  
  \[ M_{\text{ref}}(T) \triangleq \frac{dV_{\text{ref}}(T)}{dT} = - \frac{V_{\text{go}} - V_{\text{beo}}}{T_o} - \frac{\eta k (m-1)}{q} \left[ 1 + \ln\left( \frac{T}{T_o} \right) \right] + \left( \frac{2R_1}{R_2} \right) \left( \frac{\eta k}{q} \right) \ln \left( \frac{A_{j1}}{A_{j2}} \right) \]

- **Note Negative TC Of Generalized \( V_{\text{ref}} \)**

\[ V_{\text{be2}} - V_{\text{be1}} = \eta V_T \ln \left( \frac{A_{j1}}{A_{j2}} \right) \]
Bandgap Reference Design Target

- **TC Of \( V_{ref} \) Set To Zero At Temperature \( T_o \)**
  
  \[
  M_{ref}(T) \triangleq \frac{dV_{ref}(T)}{dT} = -\frac{V_{go} - V_{beo}}{T_o} - \eta k(m-1) \left[ 1 + \ln \left( \frac{T}{T_o} \right) \right] + \left( \frac{2R_1}{R_2} \right) \left( \frac{\eta k}{q} \right) \ln \left( \frac{A_{j1}}{A_{j2}} \right)
  \]
  
  \[
  \frac{V_{go} - V_{beo}}{T_o} + \eta(m-1)
  \]
  
  \[
  \frac{R_1}{R_2} = 2\eta \ln \left( \frac{A_{j1}}{A_{j2}} \right)
  \]

  \[
  \Rightarrow M_{ref}(T_o) = 0
  \]

- **Optimal Reference Voltage When \( M_{ref}(T_o) = 0 \)**
  
  - \( V_{ropt} = V_{go} @ T = T_o \)
  - Temperature Change Induces Perturbation In \( V_{ropt} \) With Respect To Bandgap Voltage (Changes Are Referenced To Bandgap Potential)

  \[
  V_{ropt} = V_{go} + \eta(m-1)V_T \left[ 1 - \ln \left( \frac{T}{T_o} \right) \right]
  \]
Bandgap Reference Circuit Performance

- **Optimal Reference Output Response**

  \[
  R_1 = \frac{V_{go} - V_{beo}}{T_o} + \eta(m-1) \Rightarrow M_{ref}(T_o) = 0
  \]

  \[
  V_{ropt} = V_{go} + \eta(m-1)V_T \left[ 1 - \ln \left( \frac{T}{T_o} \right) \right]
  \]

- **Numerical Disclosures** \((T_o = 27 \, ^\circ C)\)
  - \(T = 0 \, ^\circ C \rightarrow V_{ropt} = 1.239515 \, \text{volts}\)
  - \(T = 27 \, ^\circ C \rightarrow V_{ropt} = 1.239655 \, \text{volts}\)
  - \(T = 100 \, ^\circ C \rightarrow V_{ropt} = 1.238732 \, \text{volts}\)
    - \(\Delta V_{ropt} = 783.0 \, \mu V\) For 0 °C -To- 100 °C Temperature Excursion
    - Equivalent To A Voltage Change Of 0.0632%
    - Equivalent To A Temperature Sensitivity Of 632 ppm/°K
  - Great TC, But Low Output Voltage (Near Bandgap Of Silicon)
  - Laser Trimming Required To Set Correct Resistance Ratio, \(R_1/R_2\)
Large Bandgap Reference Output Voltage

**Circuit Schematic Diagram**
- **Design Requirements**
  - Amplifier Must Have Large Open Loop Gain To Force Identical Currents, $I$
  - Identical BJTs, Save For Area Differences
  - $TC$ Of $R_4/R_5$ And Of $R_1/R_2$ Must Be Very Small
- Resistor $R_3$ Cancels Effects Of BJT Base Currents

**Background Analysis**

\[
V_{be2} = V_{be1} + R_2 I + \left( R_2 + R_3 \right) I_b
\]

\[
V_{ref} = V_{be2} + 2R_1 \left( I + I_b \right)
\]

\[
V_A = 2R_4 I_b + \left( I + \frac{R_4}{R_5} \right) V_{ref}
\]

\[
V_{ref} = V_{be2} + \frac{2R_1}{R_2} \left( V_{be2} - V_{be1} \right) - \frac{2R_1}{R_2} R_3 I_b
\]
Large Bandgap Output Design Results

- **Modified Reference Output**

\[
V_A = \left( I + \frac{R_4}{R_5} \right) \left[ V_{be2} + \frac{2R_1}{R_2} \left( V_{be2} - V_{be1} \right) \right] \\
+ 2 \left[ R_4 - \left( I + \frac{R_4}{R_5} \right) \left( \frac{R_1}{R_2} \right) R_3 \right] I_b
\]

- **Eliminate Dependence On Base Current \( I_b \)**

\[
R_3 = \left( \frac{R_2}{R_1} \right) \left( \frac{R_4}{\parallel R_5} \right)
\]

- **Resultant Modified Reference Output Voltage**

\[
V_A = \left( I + \frac{R_4}{R_5} \right) \left[ V_{be2} + \frac{2R_1}{R_2} \left( V_{be2} - V_{be1} \right) \right] \approx \left( I + \frac{R_4}{R_5} \right) V_{ref}
\]